

Designing, building and running tracking detectors

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Outline

- Introduction
- Particle Tracking
- Why track particles?
- Silicon detector basics
- Modules
- Silicon detectors in practice
- Requirements and specifications
- Building detectors
- Designing layouts
- Realities of running detectors
- Challenges for the future
- MAPS/CMOS





Introduction

- As you will come to realise, I am a physicist working on ATLAS ITk strips
- As a result most of my examples are from ATLAS and the discussion is LHC-centric
- Have tried to concentrate on generalities of detector design
 - Dependent on exact use case, design priorities will change
 - Generally all tracking detectors aim for the same thing!
- Tried to think of the things that I wish I had been told/realised during my PhD days
- I assume everyone will have seen lectures on silicon detectors before but will anyway start with the basics
- Please feel free to stop me and ask questions at any point!!



Particle Tracking

• Particle tracking ubiquitous in particle physics from bubble chambers in the 1950s to large area tracking detectors at the LHC today







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Why track particles?

- Particle tracking allows the reconstruction of the motion of charged particles in a magnetic field
- Measurement of
 - Electric charge (direction of bend)
 - Transverse momentum (extent of bend)
 - Direction
 - dE/dx (energy loss per distance)
- Reconstruction of
 - Primary and secondary vertices
 - Impact parameters
 - Identification of τ, b etc.
 - Calorimeter impact point





Silicon detectors



- Silicon detector is "just" a reverse biased diode
- Charged particle ionises depletion layer
- Ionisation products (electrons and holes) produce a signal
 - Often called the "collected charge" (CC)



Silicon modules

- Need a way to take analogue signals from sensors and readout digitally
- Leads to the concept of the hybrid module
- ASICs designed to readout each detector
 - Typically multiple ASICs per detector due to complexity
- Combination of sensor, ASIC and any PCB circuitry referred to as a module
- Strip ASICs and sensors are connected together using wire-bonding
 - 25μ m aluminium wire ultrasonically welded to aluminium pads on sensors and ASICs
- Due to increased channel density, ASIC-sensor connection in pixels must be done using bump bonding









Strips or pixels?

- Diodes and collecting electrodes can be made "any shape you want"
- Typically two options are used:
 - 1. Approximately square sensor elements $O(100)\mu m \times O(100)\mu m "PIXELS"$
 - 2. Long, thin sensor elements O(2)cm x O(100) μ m "STRIPS"
- Each have their own advantages and disadvantages
- Pixels deployed at low radius, strips at high radius



Pixels	Strips
High resolution in both directions	High resolution in only one direction*
High data rates required to readout	Lower data rates required to readout
Lower material budget (fewer layers per space point)	Higher material budget
High power density	Low power density
Expensive when covering large areas	Effective way of covering large areas of silicon

* silicon can be processed on both sides or sensors placed back-to-back



Something in between?

 At what point do strips and pixels meet? high transverse momentum • This is the CMS upgrade PS module • Strip detector on one side with 2.5cm strips 0 • Macropixel sensor on other side with 1.5mm "macropixels" low transverse • A true hybrid module!! momentum Strip sensor Flex readout Opto-hybrid hybrid Strip readout chips (SSA) HV backplane AI-CF spacers connection Kapton isolators Power hybrid



200um thick

CF baseplate

550µm thick

CF stiffeners

Pixel chips

Pixel sensor

















Binary readout



- Typically do not readout the analogue pulse shape
- Instead read out digitally
 - Above "analog to digital conversion" just a simple comparator to a threshold voltage
 - Only information leaving the detector is a hit (1) or lack of hit (0)
 - Was there a pulse above the set threshold?
 - Sometimes can include timestamp or time over threshold (ToT) value



Thresholds





Threshold scans

- In order to understand the behaviour of the detector can perform threshold scans
 - Measure the occupancy as a function of threshold
- This can be done in three cases:
 - No injected charge ("noise occupancy")
 - Injecting a calibration charge generated within the readout ASIC
 - Injecting charge into the sensor using photons or ionising particles



A threshold scan





A threshold scan





Radiation damage

- Radiation damage can affect both sensors and readout electronics
- Bulk damage from Non Ionizing Energy Loss (NIEL)
 - Change of effective doping concentration $(\uparrow V_{dep})$
 - Increase of leakage current (个noise)
 - Increase of charge carrier trapping (\downarrow CC)
- Surface damage due to Total Ionising Dose (TID)
 - Charge build-up in oxide or Si/oxide interface ($\uparrow C_{interstrip}$)
 - Charge build up in transistors in readout chips (个noise, 个current, change in tuning)



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Radiation effects







Radiation effects





How to set the threshold

- Detector performance requirements derived from physics simulation (efficiency) and system considerations (noise)
 - Efficiency must be high enough to allow reconstruction of tracks
 - Noise must be low enough to not saturate the readout of the detector
 - Noise must be low enough to not explode the track reconstruction time
- For example, ATLAS ITk strips targets
 - Efficiency \geq 99%
 - Noise occupancy $\leq 10^{-3}$
 - Approximately maps to S:N ≥ 10:1



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Calibrating the detector





Calibrating the detector







Timing

- Importance of timing varies strongly on the detector and environment
 - Unambiguous association of a track to a given bunch crossing (25ns)
 - ≤ 30 ps can allow resolution of vertices in time enough to separate primary and secondary vertices
 - About 9mm at the speed of light
- Note that really high speed requires more "exotic" technologies such as Low Gain Avalanche Detectors (LGADs) not discussed here
- Other time-related information can be extracted:
 - Time over threshold (ToT) to measure deposited charge
 - Time stamping to measure Time of Flight (ToF)





Timing





Tracking detector requirements

- High granularity
- High data rates
- Fast response
- Low material
- High stability
- Low noise
- Low power
- Radiation tolerant
- Simple
- Cheap!!
- Easy to build
- Easy to maintain

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Technology Facilities Council The smaller the pixel size, the better the resolution:

$$\sigma^2 = \int_{-p/2}^{p/2} \frac{x^2}{p} dx = \frac{p^2}{12}$$

Fast collection time important at high rates (10s of ns)

-> Even faster response time (10s of ps) allows time-based separation of tracks for improved background rejection

Reducing material reduces multiple scattering

Lower noise means you can pick-up smaller signals

Low power means less copper needed to deliver power and less cooling required

Detector must satisfy requirements throughout lifetime

How do we build modules?

- Typically two routes to building modules
 - Industry partners
 - In house at institutes
- Productions seem big when you are in the midst of it (ITk strips contains 17,888 modules) but this is small fry to industry
- Our requirements often very different from "everyday" industry
 - Harsh radiation environment
 - 10+ year lifetime
 - Stringent quality control
 - High yield, low cost
- As a result much of production is done in house which comes with its own challenges
 - Requires high skill level personnel
 - Many institutes needed to build enough parts in the required time eg. 21 institutes world wide in 9 countries for ITk strips
 - Cross calibration of institutes (and funding agencies!) is complex
 - Many automated machines are expensive so simplicity is key
 - Have to ensure that everyone is building (and adhering) to the same specifications/procedures
 - Parts must be sent international between sites (logistics and customs!)



Module and tooling examples (glue is king!)



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What takes so long?

- The assembly and wire-bonding of modules is only a small part of the process
- Quality control and assurance take a lot of time:
 - Glue amounts/thicknesses must be checked on all modules
 - Functionality of ASICs and sensors must be tested before they are used
 - Quality of hybrids from industry must be tested before use
 - Positioning of ASICs, hybrids, sensors must be checked
 - Hybrids/modules must be tested to ensure they perform as expected
 - Hybrids go through burn-in
 - Modules go through thermal cycling
 - Subset of components get irradiated to confirm suitability
- All of this is to convince ourselves (and funding agencies) that what we are building is fit for purposes and fulfils the specifications



How do we integrate modules into a detector?

- There are multiple ways to integrate modules into a detector
 - Modules act as a standalone entity which gets integrated directly onto a structure
 - Modules get integrated onto a "local support" structure which then goes into the full structure







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Local support



- The local support concept comes into its own as the detector size increases
 - Without it, there is a power and fibre optic cable per module
 - With it, a single power/fibre connection can service a much greater area of detector



How do we service a detector?

- Bringing in services to a detector can be one of the biggest issues for material budget
 - Cooling pipes
 - Support structure (not strictly "service")
 - Power cables
 - Data cables
 - Patch panels
- It's one thing to have perfect low mass silicon detectors, it takes a lot more engineering to cool them, power them and hold them stable!





Powering

- Two main ways to reduce material in cabling
 - 1. Serial powering
 - Modules powered in series with current source
 - Total voltage required is N.V
 - "Low" current in cables results in low mass
 - BUT
 - Modules sit at different voltages which can be challenging for communication
 - Sensors typically get HV power in parallel -> V_{drop}
 - Must be a way of bypassing modules otherwise one dead module takes out many (shunts)
 - 2. DCDC powering
 - Module powered in parallel with voltage source
 - Recover resultant high current with DC-DC converters
 - Converters can have 10:1 step in V with 70% efficiency
 - Converter means "low" current in cables results in low mass
 - BUT
 - DC-DC converter is generally high mass component
 - Converter includes fast switching which can lead to noise in the module





A few words on layout

- Discussed a lot of engineering here but ultimately what we care about is physics and how tracker performance affects physics analysis
- Ultimately this comes down to simulating layouts and performing analyses on Monte Carlo to see what layouts work best
- Always a collaborative effort between the physics simulation and engineering design
- A few things to keep an eye on when designing a layout:
 - *d*₀ resolution
 - *z*₀ resolution
 - p_T resolution
 - Hemiticity
 - Tracking efficiency
 - Redundancy



$$d_0$$
 and z_0

Both improved by a low radius first layer (and optimised second layer radius)





p_T resolution

- For best p_{τ} resolution want to measure the sagitta, *S*, as well as possible
 - *p*_T = 100 GeV, *B* = 2 T, *L* = 1 m
 - *S* = 0.75 mm
- Measurement improved by
 - Strong magnetic field
 - ϕ resolution
 - Large number of hits on track
 - Minimal scattering
 - Long lever arm
 - Distance between first and last hit





A full layout





A full layout





The realities of running a detector

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Monitoring things you expected...





The realities of running a detector



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Challenges of the future

Exp.	LHC	HL-LHC	SPS	FCC-hh	FCC-ee	CLIC 3 TeV
Parameter						
Fluence [n _{eq} /cm ² /y]	N x 10 ¹⁵	10 ¹⁶	1017	10 ¹⁶ - 10 ¹⁷	<10 ¹⁰	<10 ¹¹
Max. hit rate [s ⁻¹ cm ⁻²]	100 M	2-4 G ^{****)}	8 G ^{****)}	20 G	20 M ***)	240k
Surface inner tracker [m ²]	2	10	0.2	15	1	1
Surface outer tracker [m ²]	200	200	-	400	200	140
Material budget per detection	0.3% ^{*)} - 2%	0.1% ^{*)} -2%	2%	1%	0.3%	0.2%
Pixel size inner layers [µm ²]	100x150-	~50x50	~50x50	25x50	25x25	<~25x25
	50x400					
BC spacing [ns]	25	25	>109	25	20-3400	0.5
Hit time resolution [ns]	<~25–1k ^{*)}	0.2 ^{**)} -1k ^{*)}	0.04	~10-2	~1k ***)	~5

*) ALICE requirement **) LHCb requirement ***) At Z-pole running ****) max. output rate for LHCb/high intensity flavour experiments: 300-400 Gbit/s/cm²

- Hadron colliders
 - Radiation levels ≤ 10¹⁸ n_{eq}/cm²
 - High hit rates
 - Precision timing ≤ 5 ps

- Lepton colliders
 - Small single point resolution $\leq 3 \ \mu m$
 - Very low material budget ≤ 0.2% X₀ / layer

https://cds.cern.ch/record/2649646/



(D)MAPS/CMOS?



Examples of MAPS in HEP





Want to learn more?





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🖉 Springer

