Summary of PSD13 Conference, Oxford, 4-8 Sept 2023

Chris Damerell
RAL
11 October 2023

- PSD = Position Sensitive Detectors. UK-based series with international participants, held every 3 years since 1987 (first was at UCL, triggered by the novelty of position-sensitive silicon detectors, after decades of photographic film in astronomy and particle physics – including bubble chambers and nuclear emulsions)

- Please look through the slides in areas of interest to yourself: https://indico.cern.ch/event/1230837/

- 16 categories (each with an excellent keynote speaker):
- X-ray and Gamma Ray Detectors
- Applications in Life Sciences, Biology & Medicine
- Applications in Planetary & Space Science
- Applications in Security & Environmental Imaging
- Applications in Nuclear Physics
- Applications in Particle Physics
- Applications in Astrophysics & Astroparticle Physics
- Novel Photon Detection Systems
- Detectors for Synchrotrons, FELS & other Advanced Light Sources
- Detectors for Neutron Facilities
- Detectors for High Radiation & Extreme Environments
- Advances in Pixel Detectors & Integration Technologies
- Gas-based Detection Methods
- Position Sensitive Fast Timing Detectors
- Applications in Condensed Matter
- Quantum Detectors

Total ~125 talks and posters, so I can only cover some that caught my eye.

Introductory words, an apology, and an invitation

My selection (with humble apologies for many omissions):

- Those 16 categories obscure advances which are common to most application areas, such as in the technology of silicon detectors, so I consider those first. In my opinion, the most significant advance here is in stacked CMOS image sensors, brilliantly led by SONY for optical imaging - reminiscent of the evolution of monolithic pixel devices, invented in the form of CCDs in 1970. (Physics Nobel Prize to Willard Boyle and George Smith, 2009)

- Particle physics
  - Smart pixels
  - High speed pixels, notably LGADs
  - Some thoughts on risk management

- LCLS-II at SLAC - brilliant startup on 18th September. A huge challenge for PSDs

- The advance to Ultrafast MeV-scale electron microscopy, including an initiative in the UK, and the link to attosecond laser pulses (Physics Nobel Prize to Pierre Agostini, Ferenc Krausz and Anne L'Huillier, 2023)

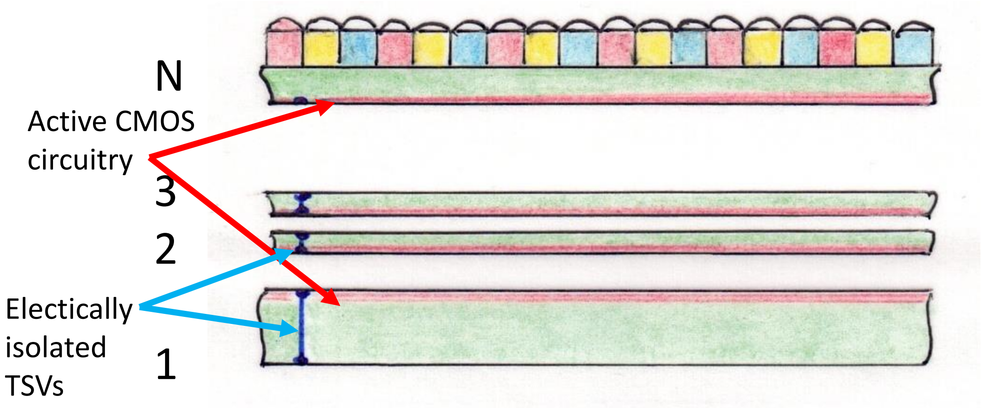
- VHE gamma ray astronomy

- Dark Matter – could it (even now) be entirely due to Primordial Black Holes?

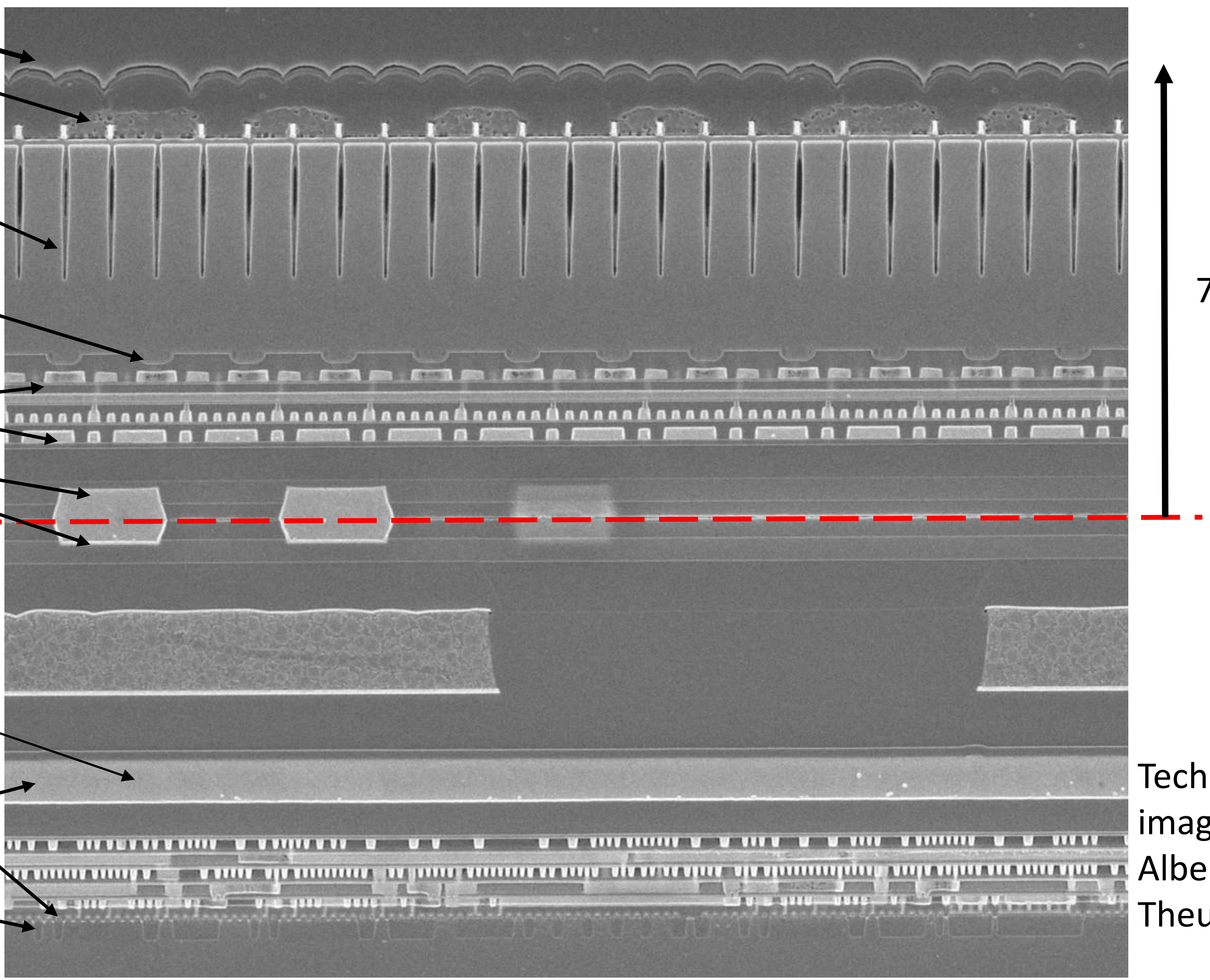
- The DM distribution of the Milky Way Galaxy (or was it a joke?)

- Stacked CMOS image sensors (layered chiplets of sensors, analog and digital signal processing, memory, ASICs, opto drivers, etc)
- For optical image stacks, use back illumination, usually but not always prefer full depletion
- Visible light and X-rays can be fully absorbed in the imaging layer, giving the stack maximum radiation hardness, while MIPs traverse the whole stack and can damage all layers
- For the simplest stack, use just 2 wafers assembled face-to-face. That's how SONY started 3 years ago …
- Technology is now moving far beyond – additional layers from different design groups, even chiplets from from different foundries working to agreed standards. Excellent crosstalk suppression – see side panel
- Intelligent in-module data processing for automotive and other real-time applications, such as signal extraction for X-ray diffraction imaging at high speed light sources such as LCLS II, or **EMERGENCY BRAKE** to vehicles.
- Don't usually need stitching, but may need 4-side buttable modules, for adequate area coverage. These are easily provided, given routine use of TSVs

Stacked CMOS image sensor (exploded view)



- Active circuitry is on top of layer 1, and on underside of all subsequent layers
- This circuitry may receive additional metal shielding, to ensure robust crosstalk suppression to the adjacent substrate after stacking (electrically clean by comparison with a complex monolithic chip)
- Note the ancient art of 'damascening' to achieve perfect planarisation for every processing step of every layer, even with many metal layers
- Once the complete module is assembled, it may be sufficiently robust mechanically for layer 1 to be further back-thinned, to minimise module thickness



micro-lenses

colour filters

DTI

Imaging Tier – pixels + front-end transistors

channel stops

Numerous metal layers

copper-copper bonds Note the wafer-to-wafer alignment! – 2 yrs

Wafer-to-wafer bond

Digital Signal Processing Tier

Note metal ground plane for inter-layer shielding (avoiding substrate currents which often induce crosstalk in monolithic devices)

numerous metal layers

transistors

7.8 µm

Tech Insights image, via Albert Theuwissen

SEM view of a slice through the imaging region of a 2-tier SONY CMOS image sensor, or CIS, with single pixel layer (CERN Courier, 2021)

Damascening

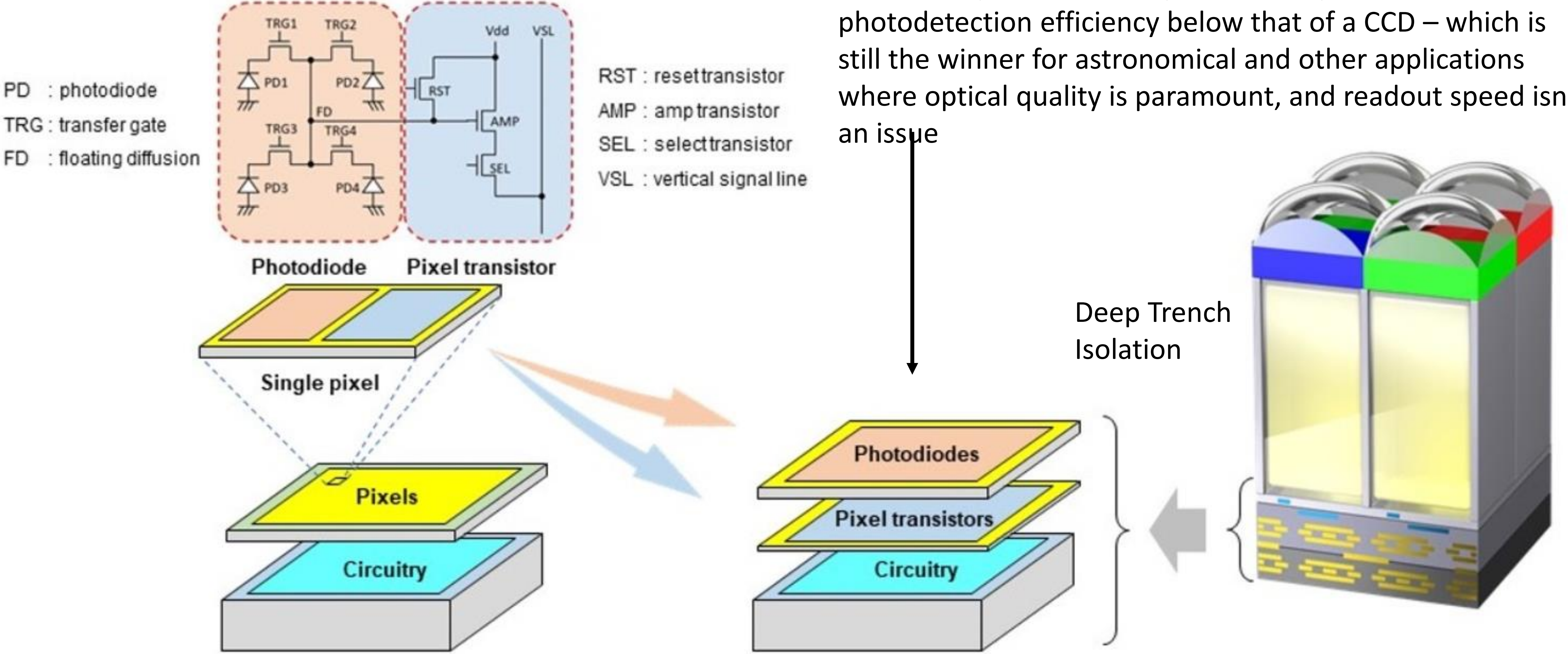
China, Warring States Period, circa 300 BC
Bronze vessel with gold and silver inlay

Toledo, Spain, 18th C
Gold inlaid in oxidized steel

- Impressive developments over past 2 years:
  - Taku Umebayashi of SONY has received the Japan Prime Minister's Award for his pioneering of stacked image sensors. He started in 2008 and 15 years later runs a group developing next-generation memory technology for these devices
  - In 2022, SONY announced the first stacked CIS with 2-layer imaging tier, comprising sense diodes and front-end transistors, which doubles saturation signal level, widens dynamic range and reduces noise (next slide)
  - There are currently 19 camera models in the world using these frontier systems, marketed by SONY, Canon and OM System. They have the fastest frame rate and highest sensitivity for visible light. They are used for many frontier applications, such as night vision systems for defence purposes
  - 90% of SONY camera output now uses stacked sensors
  - Mike Campbell reported 4-side buttable Timepix4 chips, enabled by TSVs from Fraunhofer Institute instead of wire bonds.
  - Walter Snoeys, who is developing stitched devices for ALICE with great success, knows of a company offering a foundry service for multi-chip systems which *combine* stitched and stacked devices for image sensors. This will open many doors, including for particle tracking.
  - No news at PSD13 from Grzegorz Deptuch (BNL), or Takaki Hatsui (RIKEN, who is working with SONY), in terms of stacked devices for X-ray systems, but they are advancing. There's potentially a very large market here, most urgently (I think) for LCLS II.

Quote: SONY's work ethic

Even here, presence of in-pixel circuitry reduces photodetection efficiency below that of a CCD – which is still the winner for astronomical and other applications where optical quality is paramount, and readout speed isn't an issue



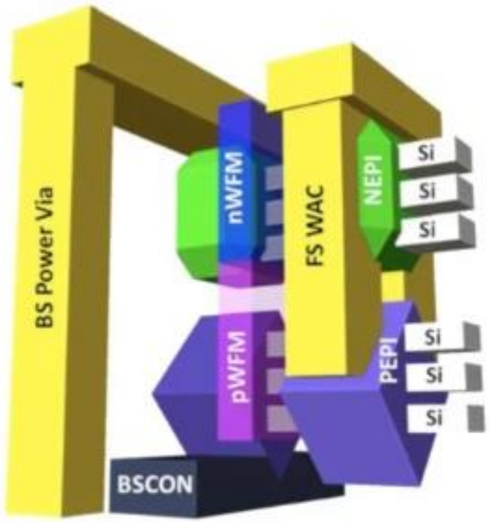
Deep Trench Isolation

Conventional stacked CMOS image sensor

Stacked CMOS image sensor with newly developed 2-Layer Transistor Pixel technology

SYNOPSYS Panel discussion: Accelerating Mainstream Adoption of Multi-Die Systems
https://www.synopsys.com/multi-die-system/accelerating-mainstream-adoption-of-multi-die-systems.html

- AKA stacked CMOS modules
- Experts in discussion from Synopsys (chair), ANSYS, Bosch, Intel, Samsung
- Example application areas: mobile devices, automotive, defence
- Functional systems: high performance computers, massive memory modules, intelligent imaging systems
- Scale of activity: 3 times more in 2023 than last year, SYNOPSYS currently tracking 100 multi-die projects world-wide
- Key challenge for the industry:
  - Need to drive standards
    - Happening *within* foundries (eg Samsung: 3d tools, 3d codes, validating processes and procedures
    - Co-operating foundries starting to define wider standards, eg UCIe:
      - Universal Chiplet Interconnect Express is an open specification for a die-to-die interconnect and serial bus between chiplets. It is co-developed by AMD, Arm, ASE Group, Google Cloud, Intel, Meta, Microsoft, Qualcomm, Samsung, and TSMC.
    - In China, they have recently agreed standards between many companies within their automotive eco-system
- General enthusiasm for moving from a chip-centric to a system-centric view - it's just beginning.



Intel, TSMC both set to report on stacked CFETs at IEDM

Technology News | October 3, 2023

By Peter Clarke

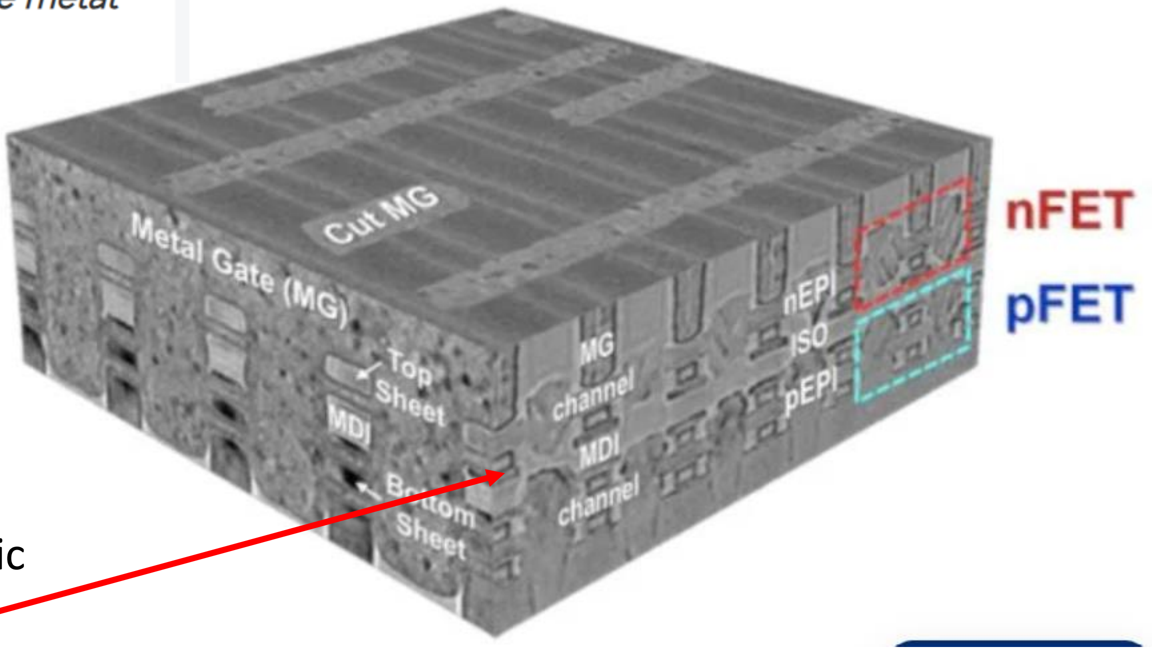
TSMC's monolithic CFET with a gate pitch of 48nm and with nFETs placed above pFETs, and both types of transistors surrounded by a single metal gate. Source: IEDM.

IEDM 69th International Electron Devices Meeting

9-13 Dec, 2023

Complementary field-effect transistor (CFET) is a future transistor type with a high potential to be used beyond 3-nm technology nodes

On-state current and subthreshold leakage: on/off current ratio = 10^6



Middle Dielectric Isolation (MD)

FUTURE OF COMPUTING CONFERENCE

Enhanced Performance Through Advanced Materials

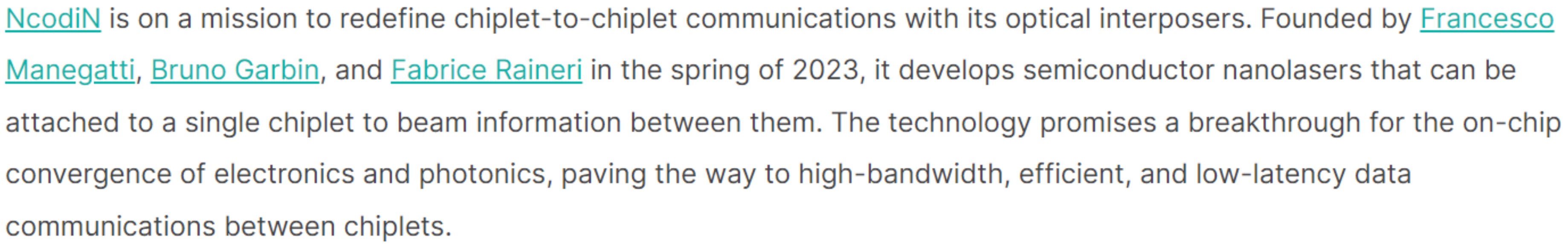
28 November 2023

Estrel Convention Center, Berlin

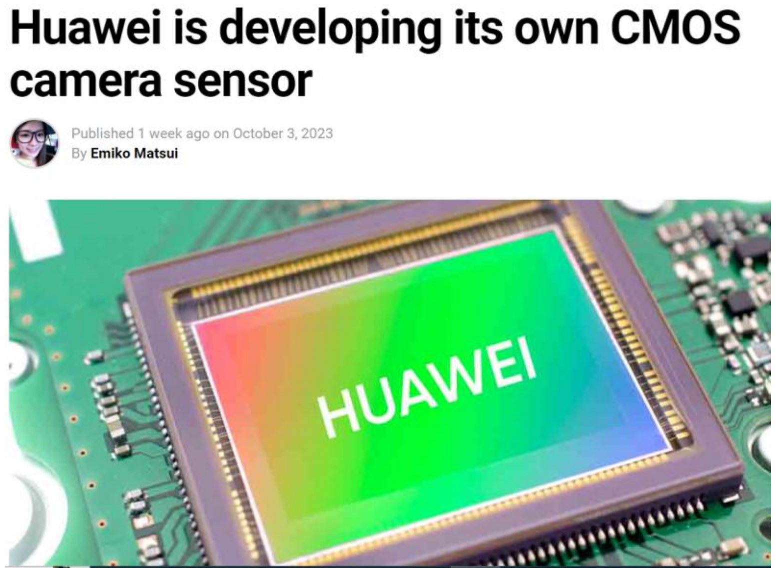
Visit www.future-of-computing.eu to learn more.

NcodiN

Illuminating the future of computing



NcodiN is on a mission to redefine chiplet-to-chiplet communications with its optical interposers. Founded by Francesco Manegatti, Bruno Garbin, and Fabrice Raineri in the spring of 2023, it develops semiconductor nanolasers that can be attached to a single chiplet to beam information between them. The technology promises a breakthrough for the on-chip convergence of electronics and photonics, paving the way to high-bandwidth, efficient, and low-latency data communications between chiplets.



Huawei is developing its own CMOS camera sensor

Published 1 week ago on October 3, 2023

By Emiko Matsui

Huawei and Sony:

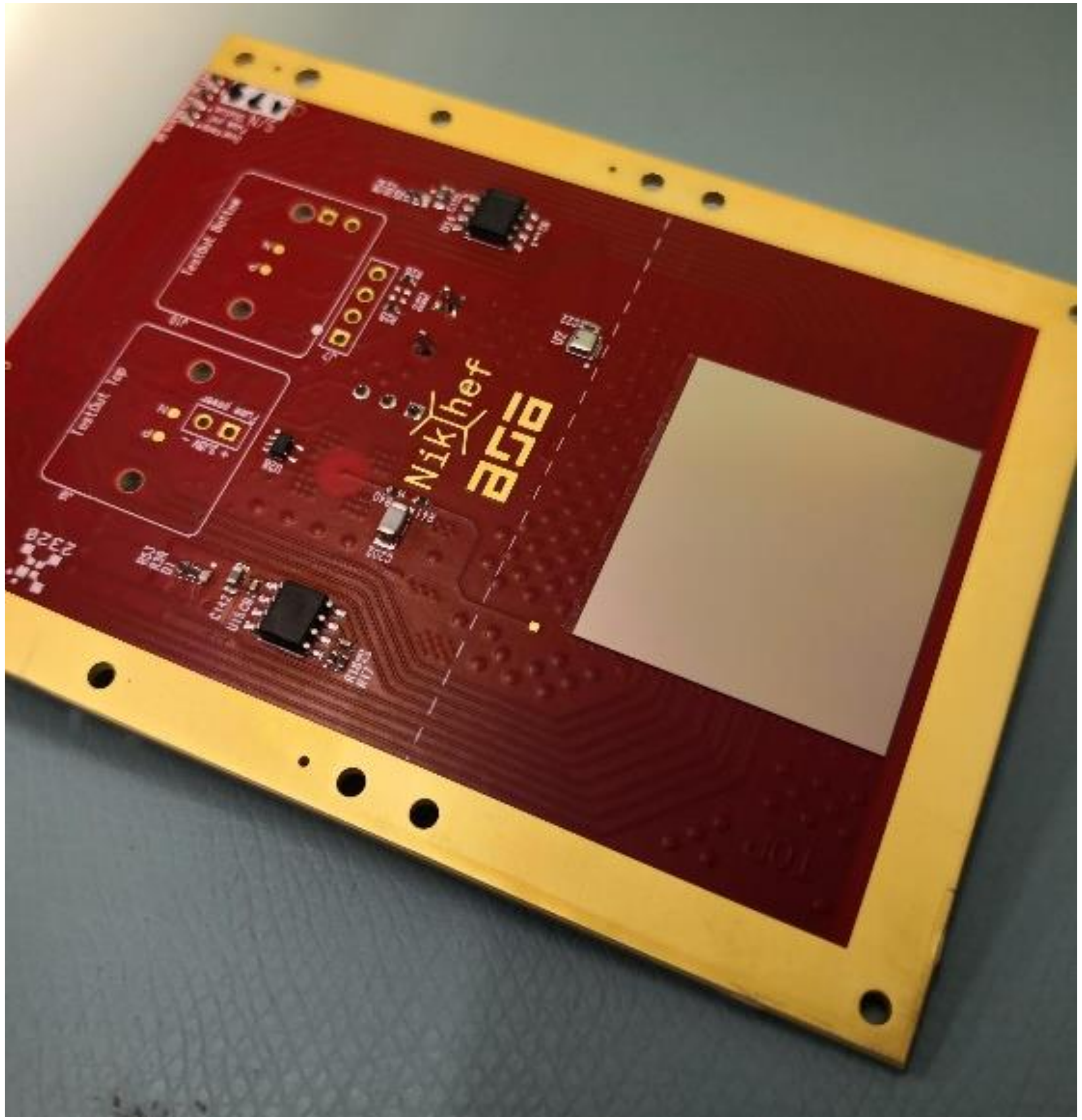
Sony and Huawei have been working together on camera sensor technology for a long time. After US sanctions, Sony received permission to supply image sensors to Huawei. However, the Chinese techmaker is now working more on itself rather than relying on Sony for its mobile camera requirements.

Your next Samsung phone could have a whopping 432MP camera

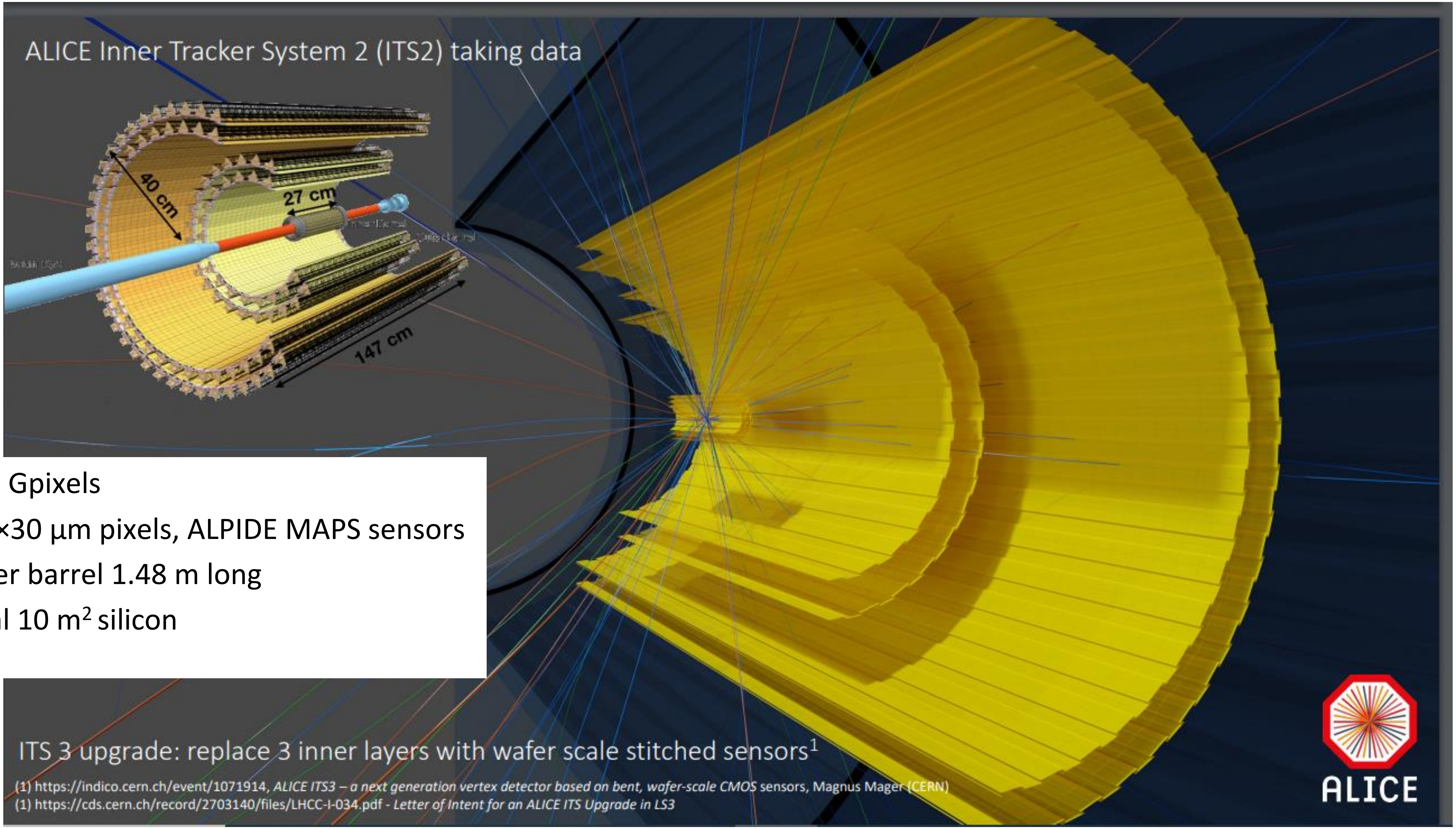
According to the report, the sensor will be one inch across, and could feature 36:1 pixel binning. That could mean unimaginably good low light performance, with 36 pixels doing the job that would previously have been done by one.

TSV-processed successfully mounted

Michael Campbell



Chip behaves identically to a wire bonded version. But the TSV version is 4-side buttable



ALICE Inner Tracker System 2 (ITS2) taking data

ITS 3 upgrade: replace 3 inner layers with wafer scale stitched sensors[1]

(1) https://indico.cern.ch/event/1071914, *ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS* sensors, Magnus Mager (CERN)
(1) https://cds.cern.ch/record/2703140/files/LHCC-I-034.pdf - *Letter of Intent for an ALICE ITS Upgrade in LS3*

- 12.5 Gpixels
- ≈30×30 µm pixels, ALPIDE MAPS sensors
- Outer barrel 1.48 m long
- Total 10 m^2 silicon

Walter Snoeys

[ITS3 "engineering model 1" made of 3 layers of dummy silicon, 40-50 µm thick]

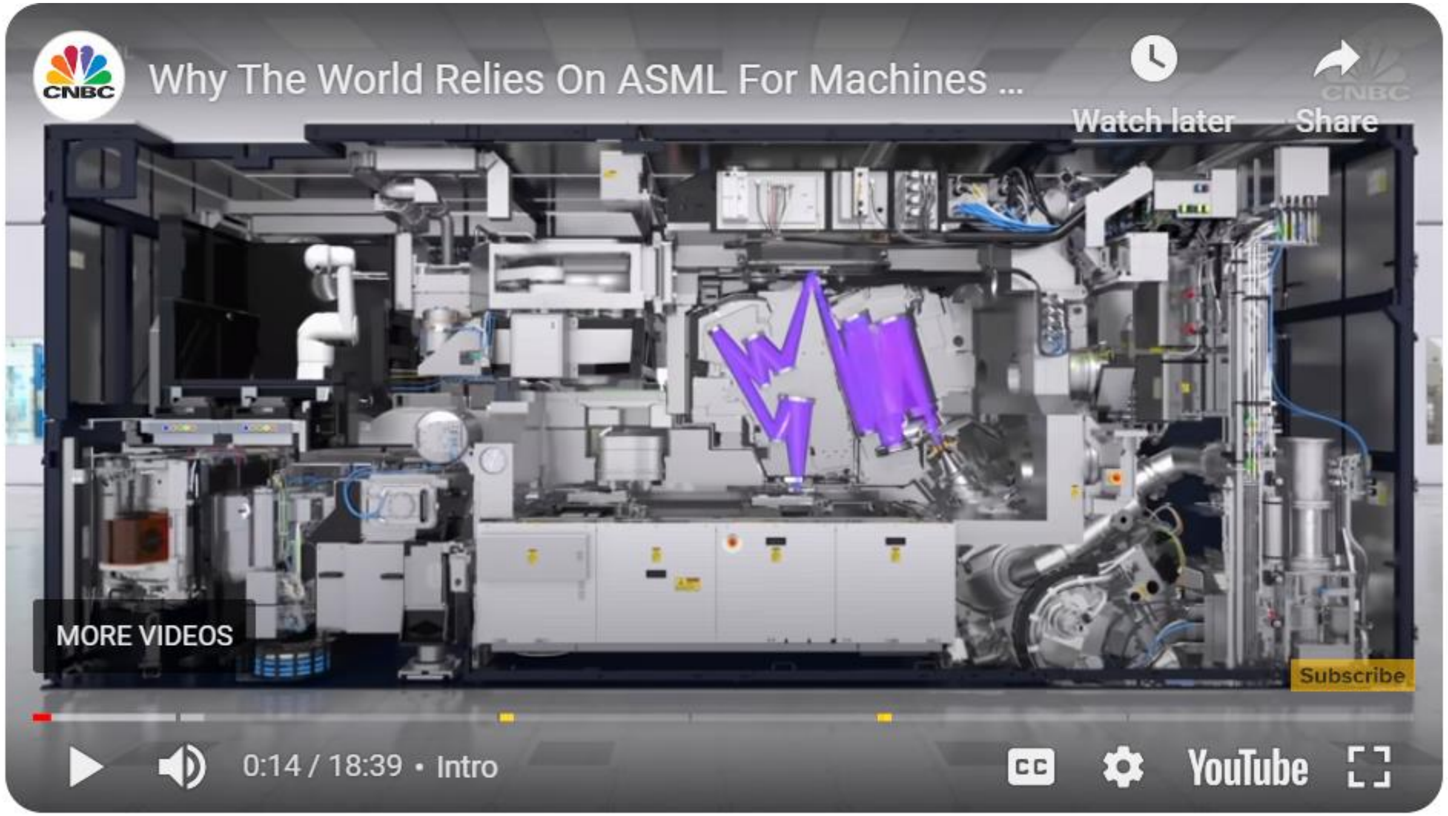
ITS3. Curved wafer scale stitched CMOS sensors, huge pioneering effort of ALICE Collaboration.
Sensors use TPSCo 65 nm process, Collaboration led by CERN Microelectronics (Walter Snoeys)

12" (300 mm) diameter wafers suffice for these half-cylinders. 65 nm is sufficient: far below state-of-art in wafer processing, which is pushing 2 nm effective feature size, measured by transistor density

Excellent YouTube - EUV wafer processing machine from ASML in Netherlands (outgrowth from Philips)

https://www.youtube.com/watch?v=iSVHp6CAyQ8

- λ = 13.5 nm, beyond DUV, λ = 193 nm
- EUV needed for effective feature size below 14 nm, down to 2 nm (measured by density transistors)
- 30 component machines gathered together from ASML subsidiary companies world-wide
- Assembled and commissioned in Netherlands, then disassembled and shipped to the customer
- 20 trucks, 3 Boeing 747 transport planes, at cost of $200M
- ASML expect to complete delivery of 30 units during 2023
- Export to China is currently blocked. So …



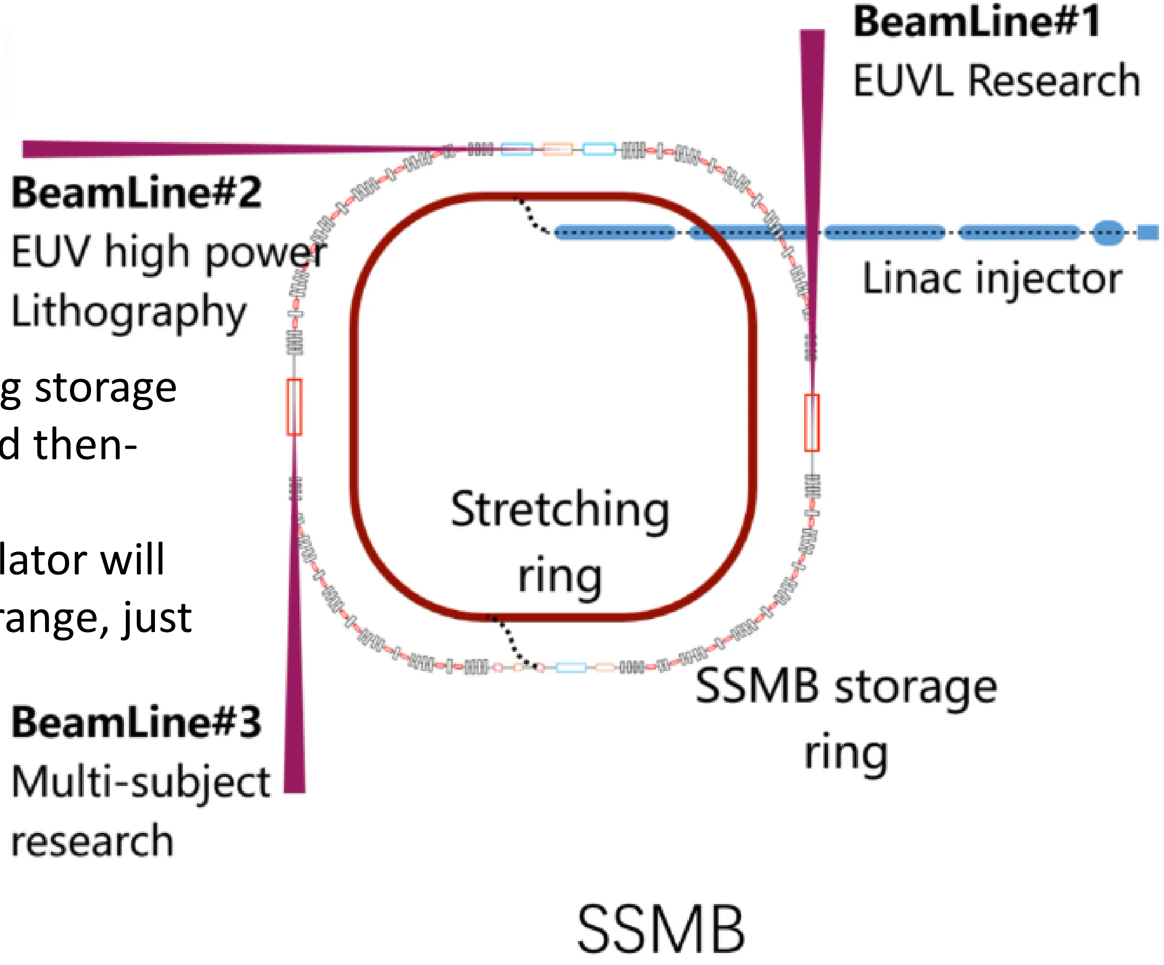
Size of a
large truck

Article in South China Morning Post
https://www.scmp.com/news/china/science/article/3235419/china-plans-build-giant-chip-factory-driven-particle-accelerator

Prof Tang Chuanxiang
Of Tsinghua U

‘Many lithography machines’

SSMB – Steady State Microbunching storage ring, proposed by Prof Zhao Wu and then-student Daniel Ratner, SLAC 2010. Circumference ~100 m. Each undulator will produce SR light down to the EUV range, just short of X-rays

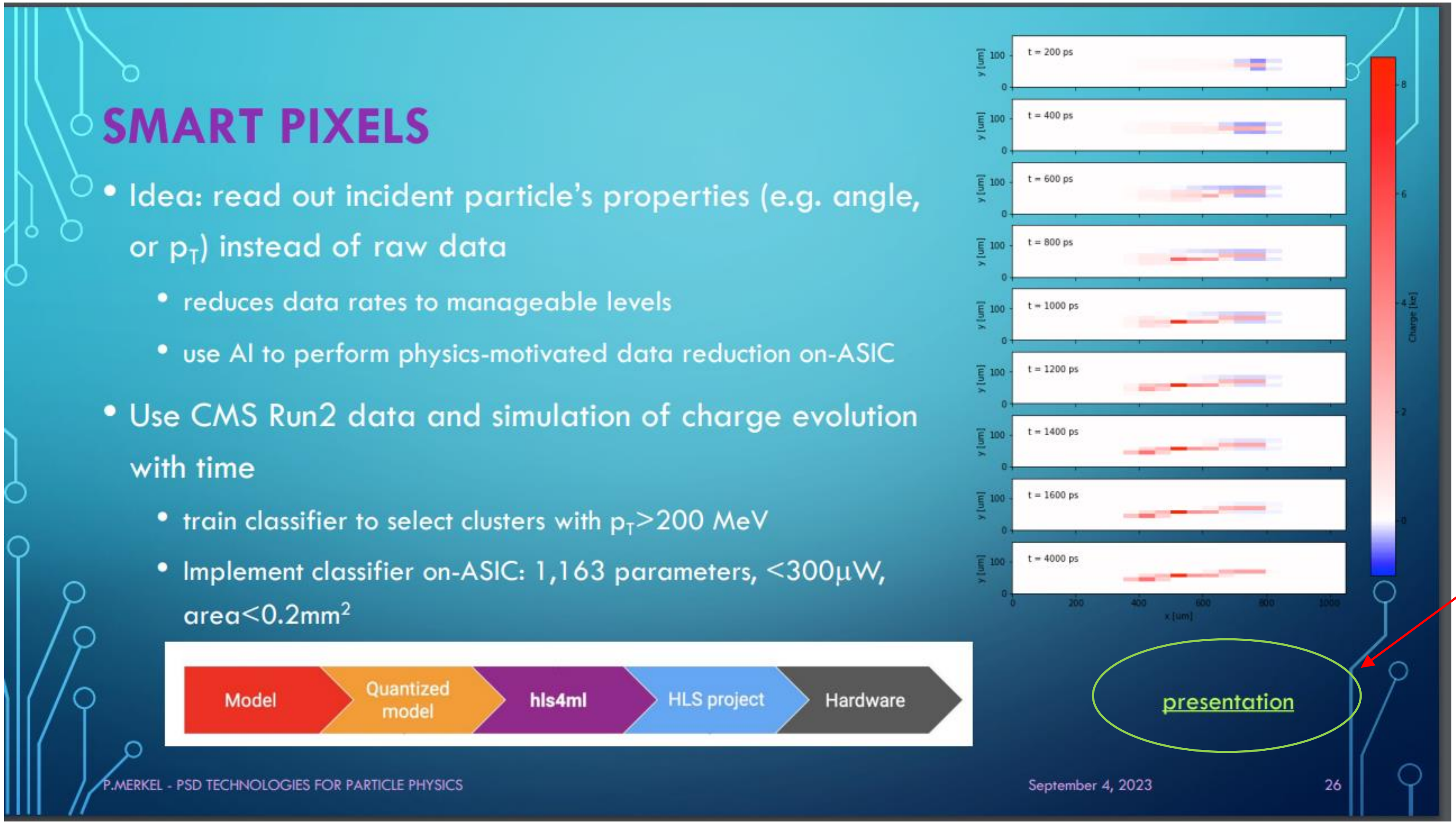


How the Tsinghua SSMB-EUV light source works. Photo: Tang Chuanxiang

‘Compared with current ASML EUV technology, SSMB will be a more ideal light source. It will have a higher average power and higher chip production output with lower unit cost.’

100 W to 1 kW on wafer, compared to 5 W ASML

- Petra Merkel's Keynote talk – Particle Physics
- Links to a presentation of Jennet Dickinson at Fermilab.
- Assumes 28 nm CMOS, and a stacked architecture could possibly enable even more challenging applications than HL-LHC, notably FCC-hh



SMART PIXELS

- Idea: read out incident particle's properties (e.g. angle, or p_T) instead of raw data
  - reduces data rates to manageable levels
  - use AI to perform physics-motivated data reduction on-ASIC
- Use CMS Run2 data and simulation of charge evolution with time
  - train classifier to select clusters with p_T>200 MeV
  - Implement classifier on-ASIC: 1,163 parameters, <300μW, area<0.2mm^2

Model → Quantized model → hls4ml → HLS project → Hardware

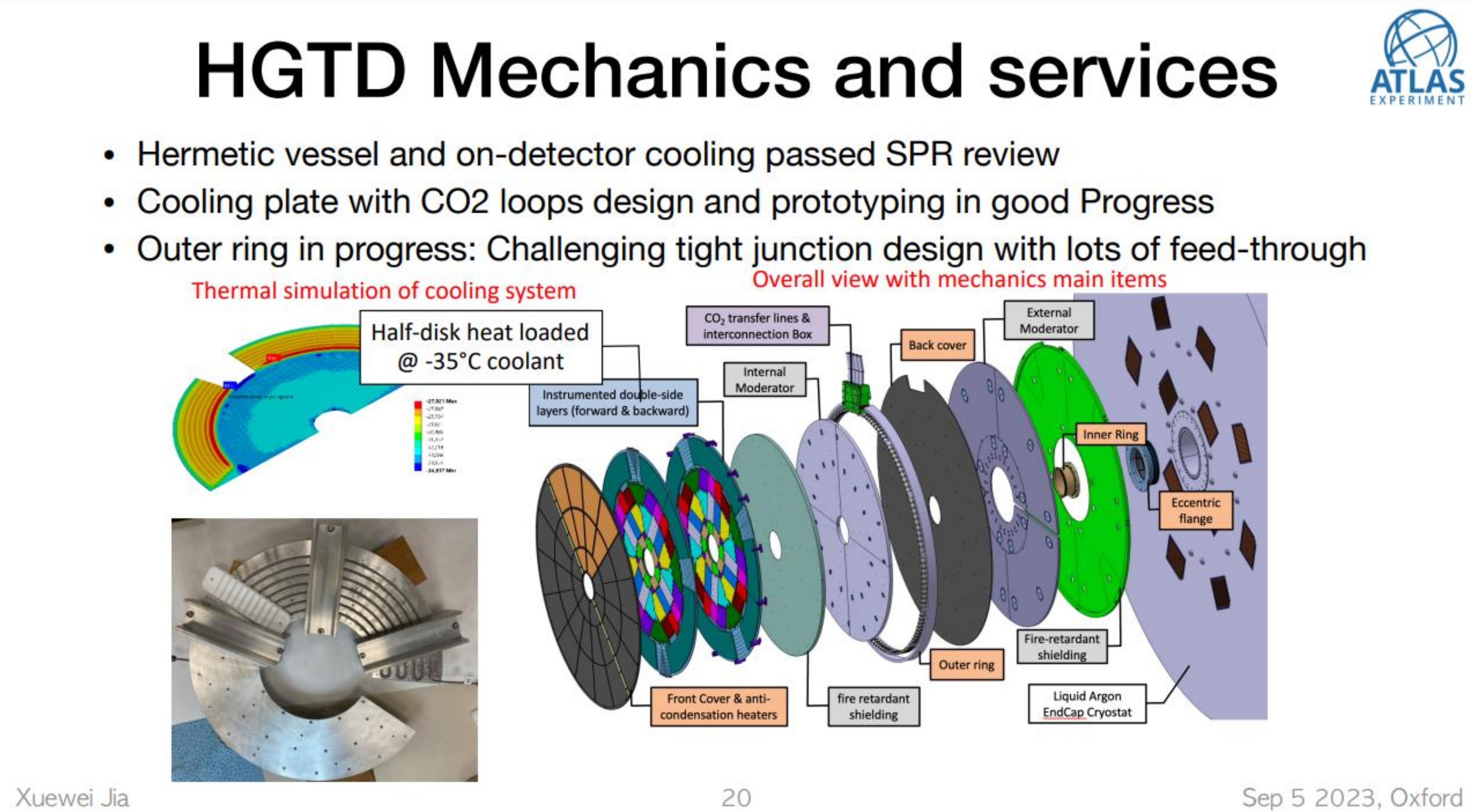
presentation

P.MERKEL - PSD TECHNOLOGIES FOR PARTICLE PHYSICS

September 4, 2023

26

- For HL-LHC, ATLAS (High Granularity Timing Detector - below) introduce large pairs of LGAD disks between the barrel tracker and ECAL, for pileup suppression by point measurements on all seen tracks, with 1.5 mm square pixels, 30-50 ps timing precision
- Carbon enrichment enhances the rad hardness
- SEB – Single Event Burnout is a nasty problem – avoided by restricting the operating voltage
- 3 Chinese companies will provide the full system of LGADs. Start full production next year
- Readout with 130 nm CMOS ASICs from TSMC, bump-bonded



HGTD Mechanics and services

- Hermetic vessel and on-detector cooling passed SPR review
- Cooling plate with CO2 loops design and prototyping in good Progress
- Outer ring in progress: Challenging tight junction design with lots of feed-through

Thermal simulation of cooling system

Half-disk heat loaded @ -35°C coolant

Overall view with mechanics main items

Xuewei Jia   20   Sep 5 2023, Oxford

‘Everyone makes mistakes’ – Risk Analysis and Risk Management Procedures

‘Incidents’ are generally resolved, but are sometimes accompanied by a reluctance to talk about them in public, so important lessons may not be shared. Some projects are simply abandoned, as happened with UA1 after the ‘room temperature calorimetry’ disaster

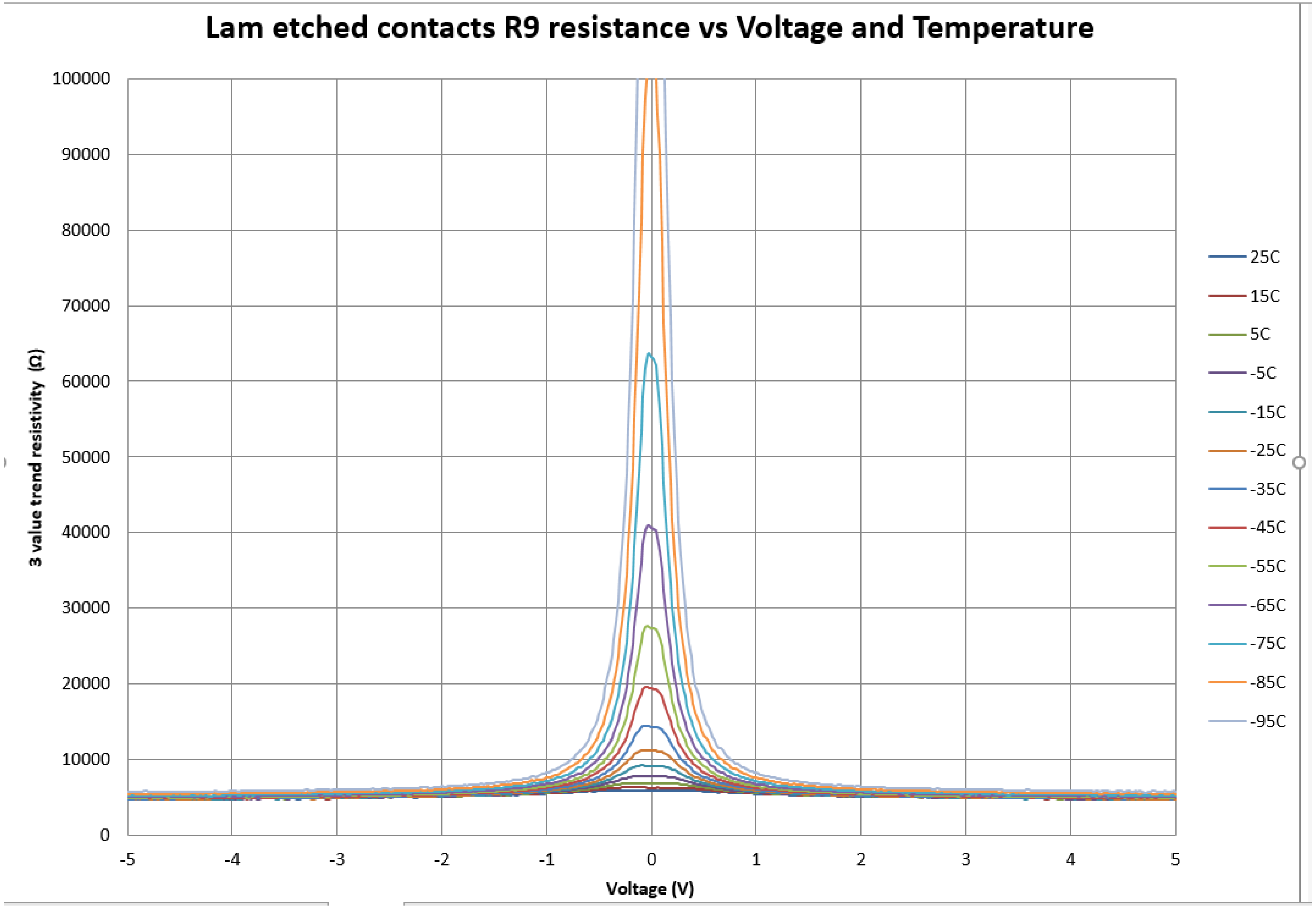
A few examples:

- The first attempt to get min-I signals from silicon pixel detectors (CCDs) in the t6 beam at the CERN PS, 1979
- The failure of LHC splice joints during commissioning
- The failure of the first production CCDs for LSST (eventually 3.2 Gpixels of highest quality)
- The ‘vacuum incident’ with the LHCb RF box (this conference)

Lessons learned:

- Rigorous procedures that were followed for 20 years at CERN, RAL and SLAC, with no further incidents *of that type*
- Rigorous procedures under the guidance of an enlightened Director
- Switch to a balanced investigative procedure for both design *and production*
- Not discussed at PSD13 – just ‘replace the box’, but presumably robust procedures in future. Is there a report on this?

- LSST CCD prototyping went smoothly from ~2010, but in 2014 production was held back for a year due to a DOE funding freeze. Then in 2015, e2V were unable to produce working devices.
- Weekly crisis meetings focused on possible ‘design improvements’. Why only that?



Vacuum incident

Failure of the LHC vacuum control system.

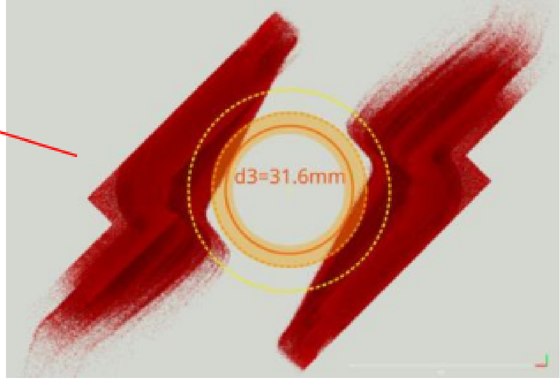
Plastic deformation of the RF foil.

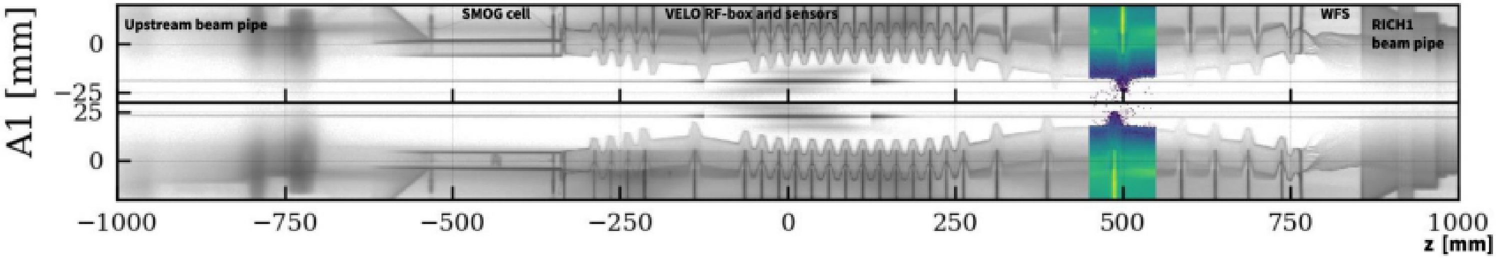
Pumping action into primary vacuum:
- Resulted in 200 mbar pressure on the RF foil
- Designed to withstand 10 mbar

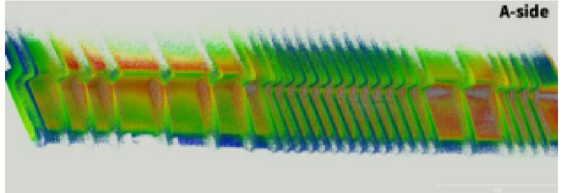
Recovery:
- Simulation and tomography to reconstruct the deformation
- Affects VELO movement
- VELO partially open until RF foil replacement in 2024

The tomography

- Radius reduced from 49 to 31.6 mm
- SMOG 2 injection to increase the production of particles outside the interaction region
- Dataset taken on 7.8 TeV
- Events of at least 3 displaced tracks taken into account







U of Science and Technology, Cracow

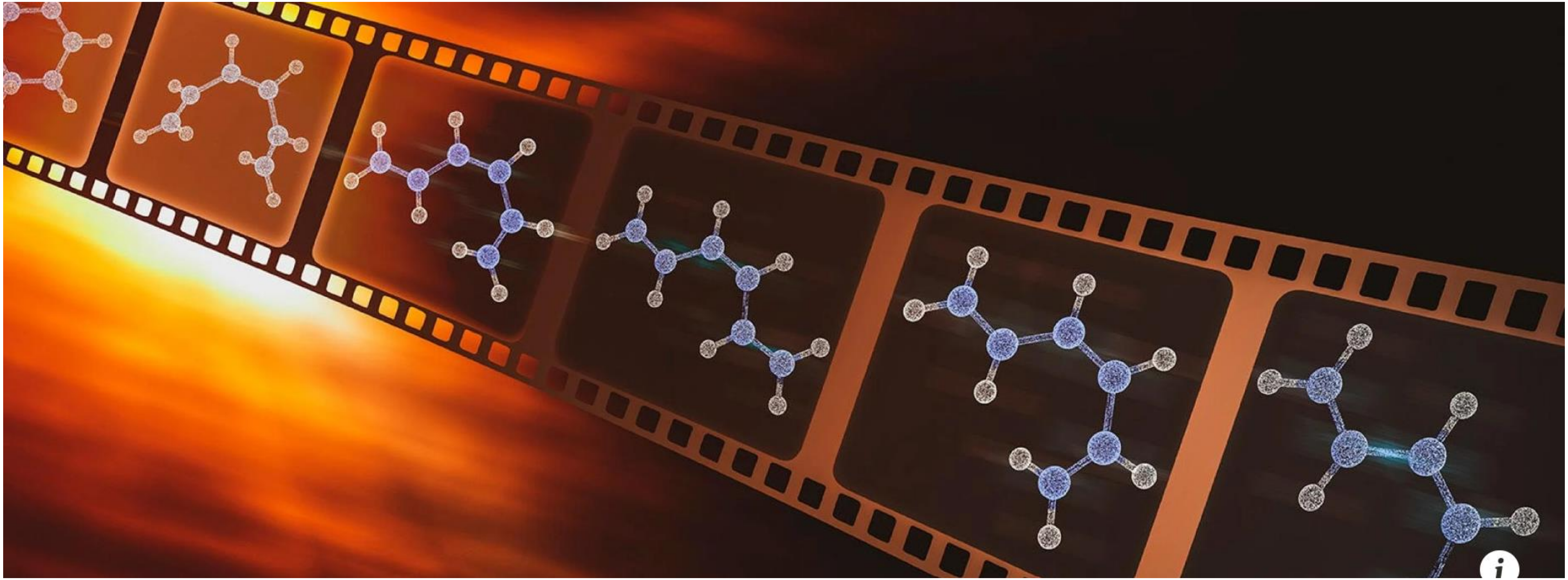
Celebrating the startup of LCLS-II, 18th Sept 2023. Collaboration between SLAC, Fermilab, Jlab, …

https://www6.slac.stanford.edu/news/2023-09-18-slac-fires-worlds-most-powerful-x-ray-laser-lcls-ii-ushers-new-era-science

LCLS operates with an X-ray bunch frequency of 120 Hz. Comparable to the EUXFEL average, but far below the needs of science

LCLS-II operates continuously at 1 MHz. Wonderful for science, but a huge challenge for the detectors

Pief Panofsky, Stanford U 1962, convincing the trustees to go for the 2-mile monster. Expected lifetime? …



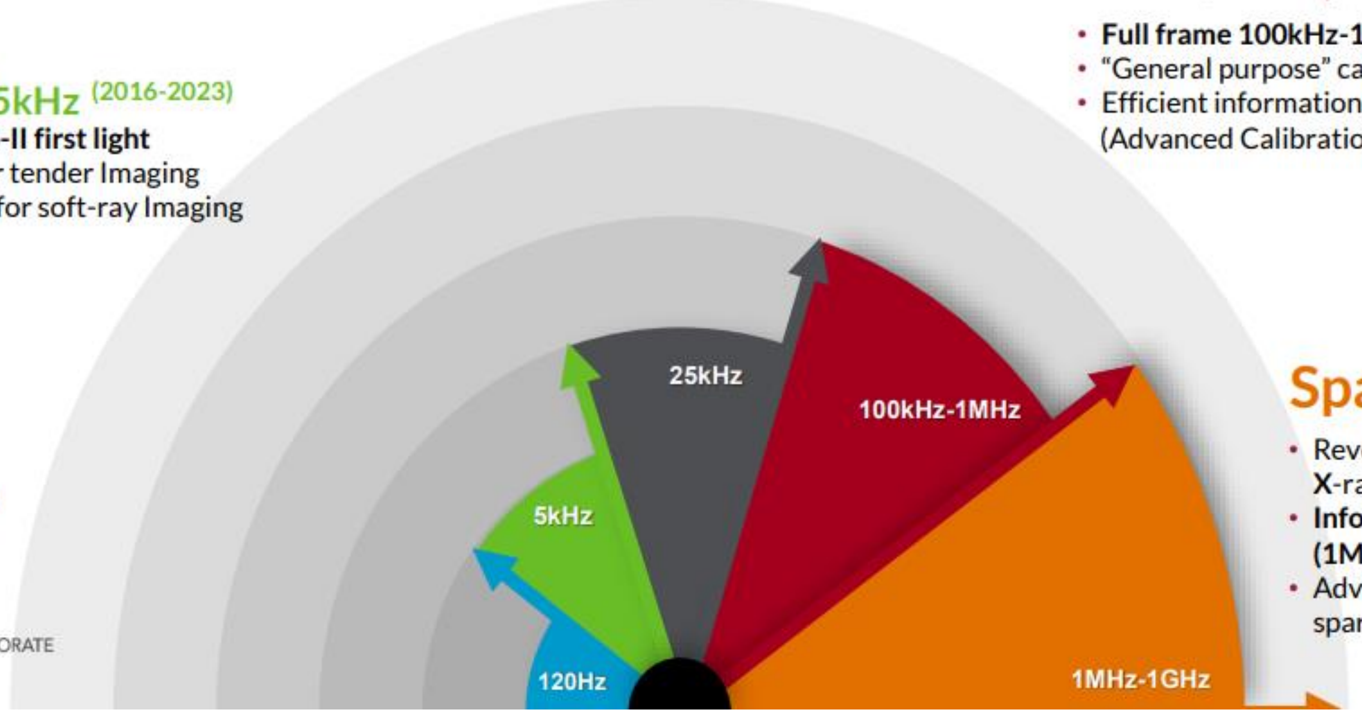
Beautiful simulations of ‘molecular movies’, which will enable breakthroughs in vast areas of science including photosynthesis and retinal functions, by observing molecules responding to optical stimulation, femtosecond by femtosecond, pumped with short flashes of light (this year’s Nobel Prize for physics) and probed by short bursts of X-rays from LCLS-II

Huge challenge for experiments and detectors, aiming eventually for studies with single molecules (spi – single particle imaging). ‘Diffraction before destruction’

SLAC long-term X-ray detector development plan

Bigger, Faster, Higher resolution and Higher Energies

With goals built into projects progressively meeting science priorities and requirements



ePixUHR$_{35kHz}$ (2019-2027)
- **Full frame 35kHz for HE first light**
- Sensors for hard X-rays

ePixUHR (2019-2029)
- **Full frame 100kHz-1MHz**
- "General purpose" cameras
- Efficient information extraction (Advanced Calibration / Edge-ML)

ePixHR$_{5kHz}$ (2016-2023)
- **5kHz for LCLS-II first light**
- ePixHR10k for tender Imaging
- ePixHR250M for soft-ray Imaging

SparkPix (2020-2027)
- Revolutionary **E**xperiment **S**pecific **X**-ray **C**ameras
- **Information extraction at full rate (1MHz CW, 3GHz burst)**
- Advanced features (triggering, sparsification, zero suppression etc.)

ePix (2013-2018)
- **In use at LCLS**

SLAC TECHNOLOGY INNOVATION DIRECTORATE

- Looks like a natural area for stacked modules – with layers of ASICs for triggering and data sparsification

- Large area detectors – 4-side buttable a must

- Timescale? Expect surprises from SONY and their collaborators? Any news from next month's CPAD conference?

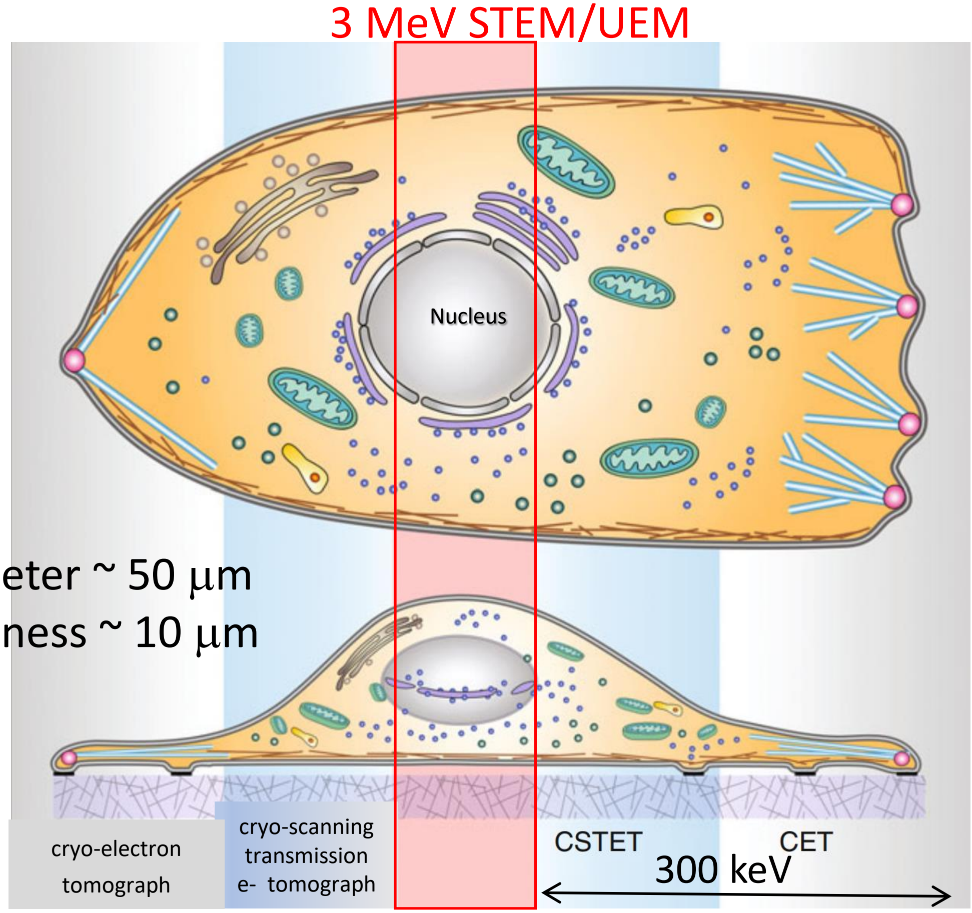
Coordinating Panel for Advanced Detectors (CPAD) Workshop
November 2023, SLAC National Accelerator Laboratory
https://indico.slac.stanford.edu/e/cpad2023

[Very good talk last year from Ron Lipton]

Promise of MeV Microscopy

Benefit of increasing electron energy to MeV

- **Life science application**: 3D image intact thick bio-samples
- No need of cryo-FIB (focused ion beam) slicing thick cells
- Limit to 10-20 lamellae/day, "blindly" select target
- Speed up discovery

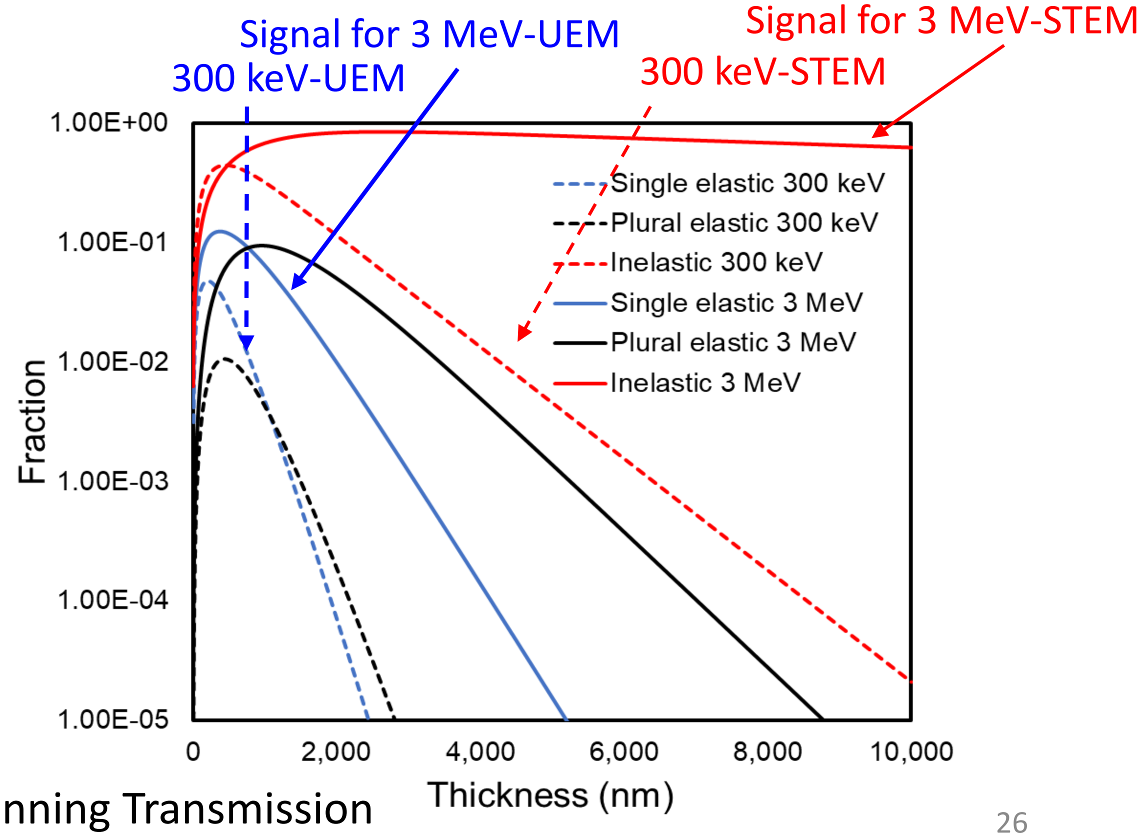


Diameter ~ 50 µm
Thickness ~ 10 µm

Top and side views of a eukaryotic cell.

S.G. Wolf, et al., Cellular Imaging, Springer

- Why MeV? Phase contrast (TEM) & amplitude contrast (STEM)
- 300 keV
  - Single-elastic drop <1% after 1-µm ice layer
  - Inelastic drop <1% after 4-µm
- 3 MeV
  - Single-elastic drop <1% after 2-µm ice layer
  - Inelastic stays 63% after 10-µm

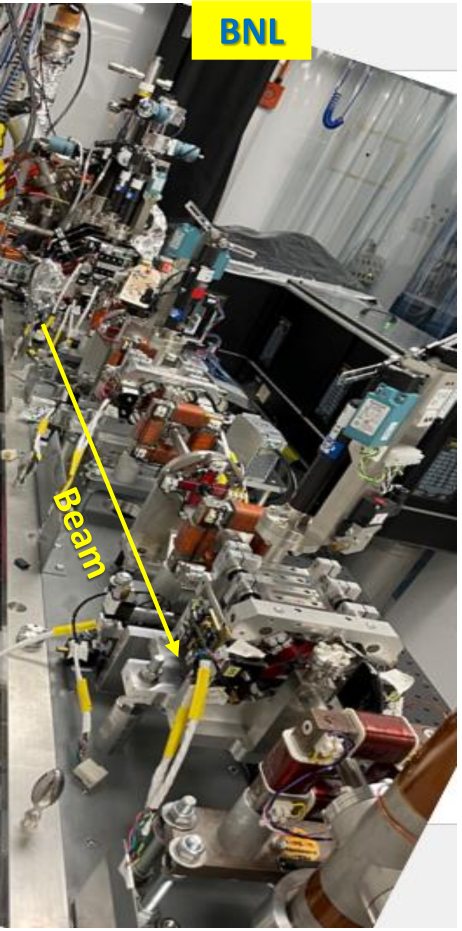


STEM Scanning Transmission Electron Microscopy

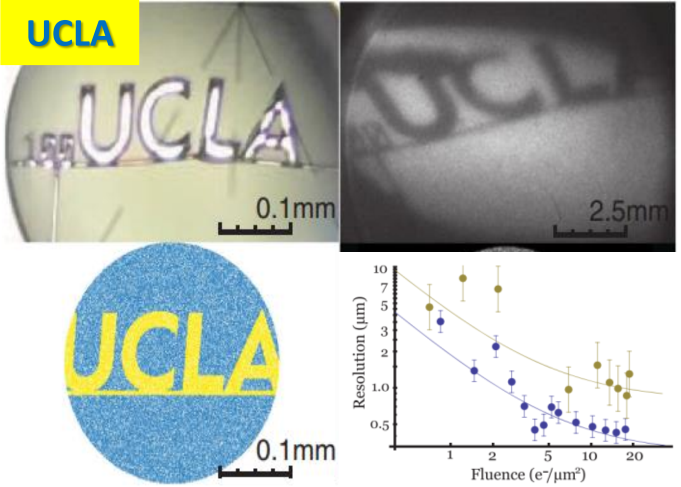
State of art MeV UEM/UED: world-wide efforts

A UK Facility for Relativistic Ultrafast Electron Diffraction & Imaging (RUEDI)

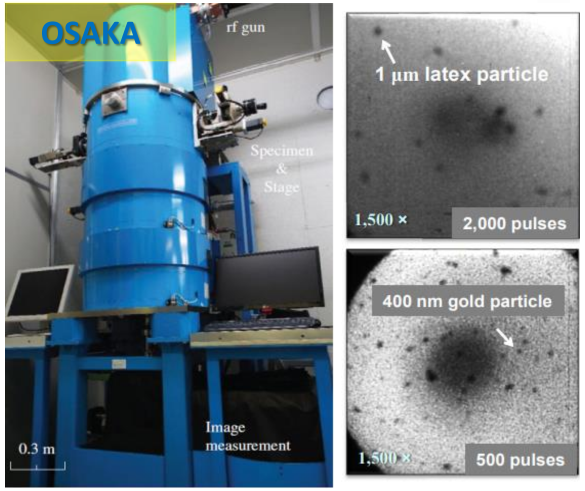
‘Beam’ could be 1 cell of a C-cubed structure



Wait for beam testing

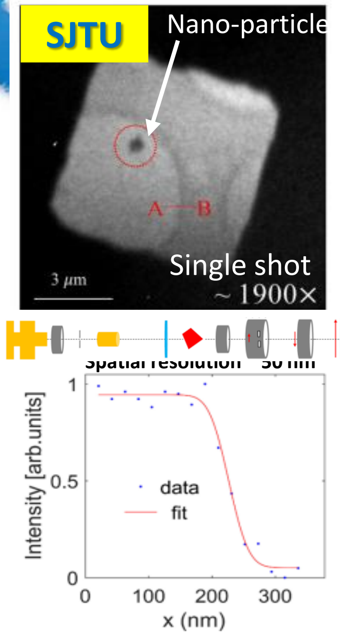


PRL 118, 154802 (2017)



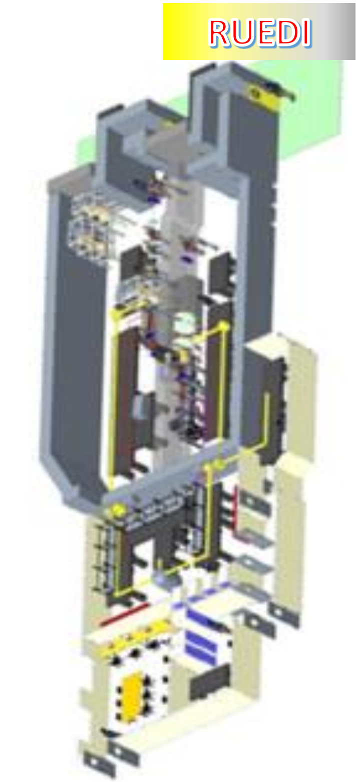
Temporal resolution 180 fs

Microscopy 67, 291 (2018)



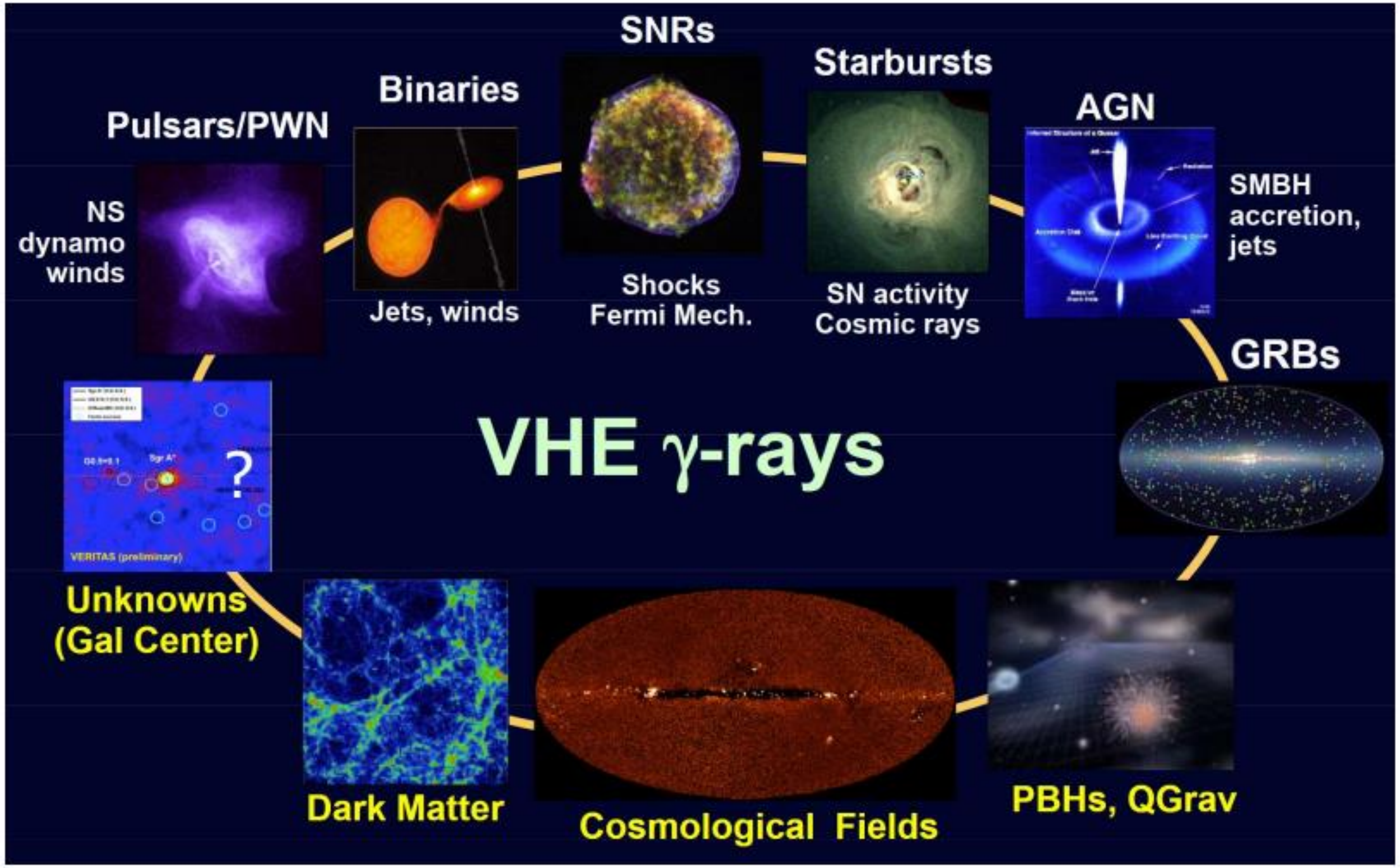
$E = 3MeV, \frac{\Delta E}{E} = 5 \cdot 10^{-4}$

Appl. Phys. Lett. 112, 113102 (2018)



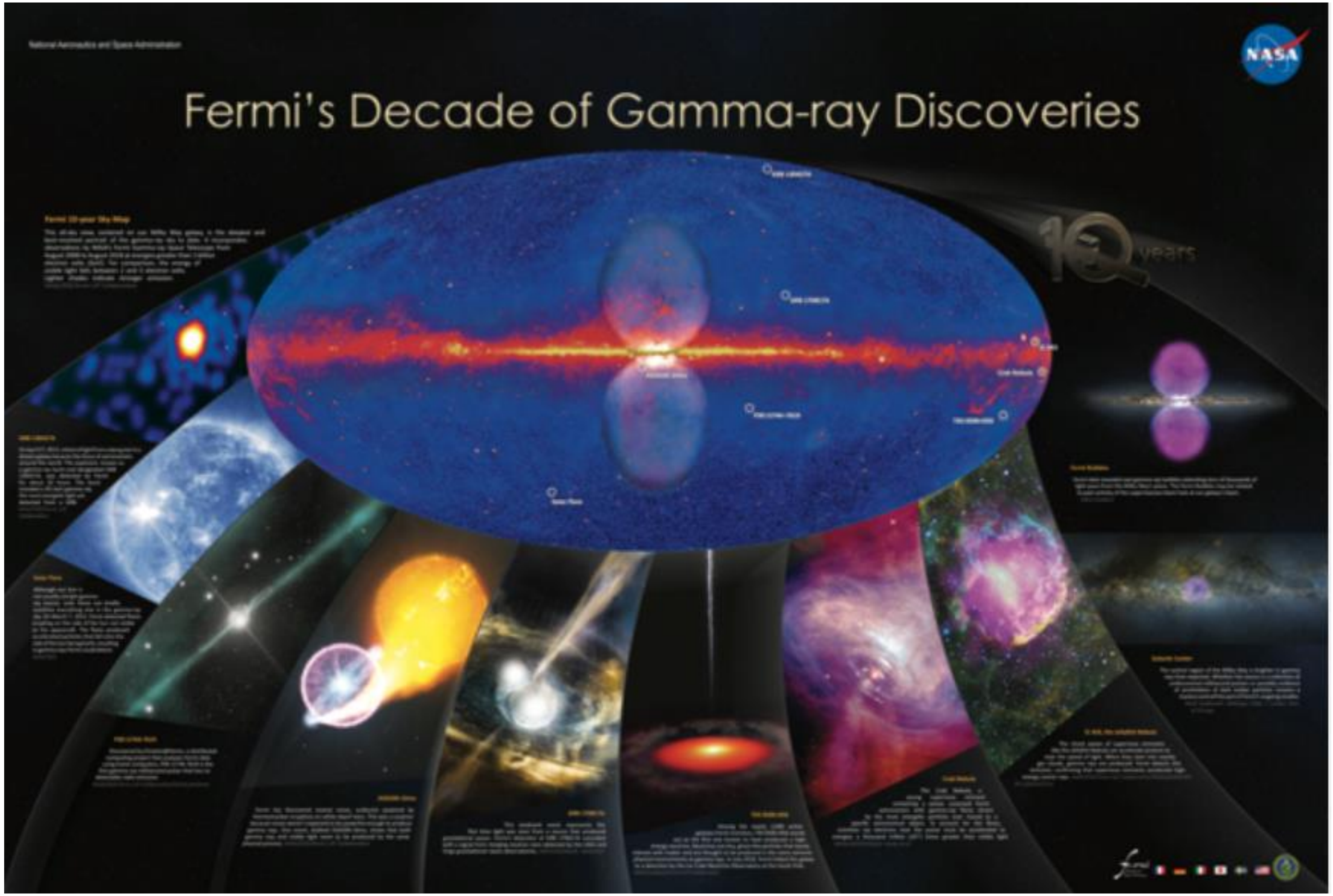
proposed UK National User Facility halfway through design stage

Why do VHE Gamma-ray astronomy?



Jon Lapington, Leicester U

- Light, gamma rays and neutrinos point back to the source. Charged particle cosmic rays are curved by magnetic fields
- Very High Energy gamma rays must have interesting origins
- Need large effective area, so not possible from space. Natural detector, the earth's atmosphere



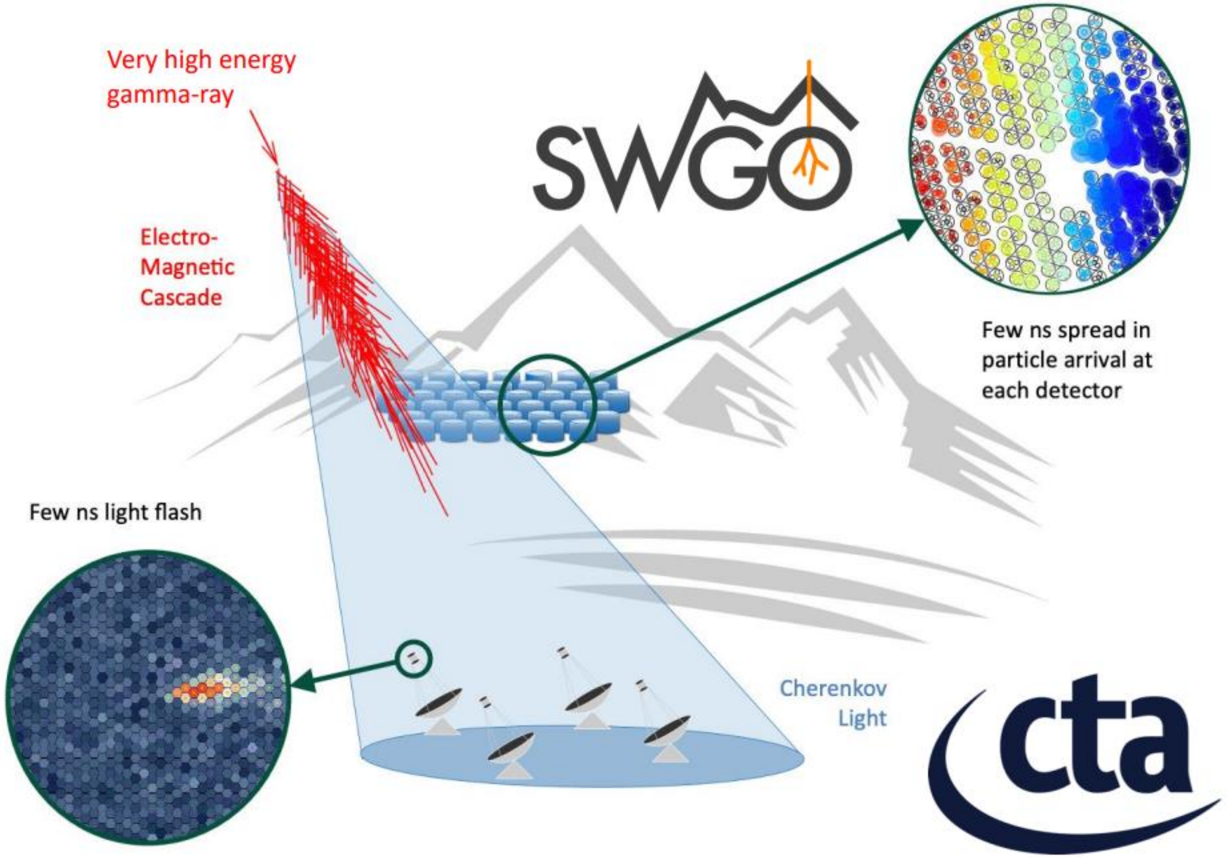
- Formerly GLAST, renamed Fermi Gamma Ray Space Telescope
- Operating since 2008
- γ-ray energies 8 keV to 300 GeV, above which statistics is minimal and energy measurement is partial
- Fermi bubbles and many major discoveries related to neutron stars, black holes and other scenes of violent jets
- Broadly international, but not UK

- 2 big ones on the way, the Southern Wide-Field Gamma Ray Observatory, and the Cerenkov Telescope Array Observatory (North and South)
- Key features are:
  - high altitude. Shower max is at ~10 km altitude
  - large area coverage, to accumulate good event samples up to PeV range
- Both will deliver a factor more than 10 increase in high energy events over the total from existing telescopes

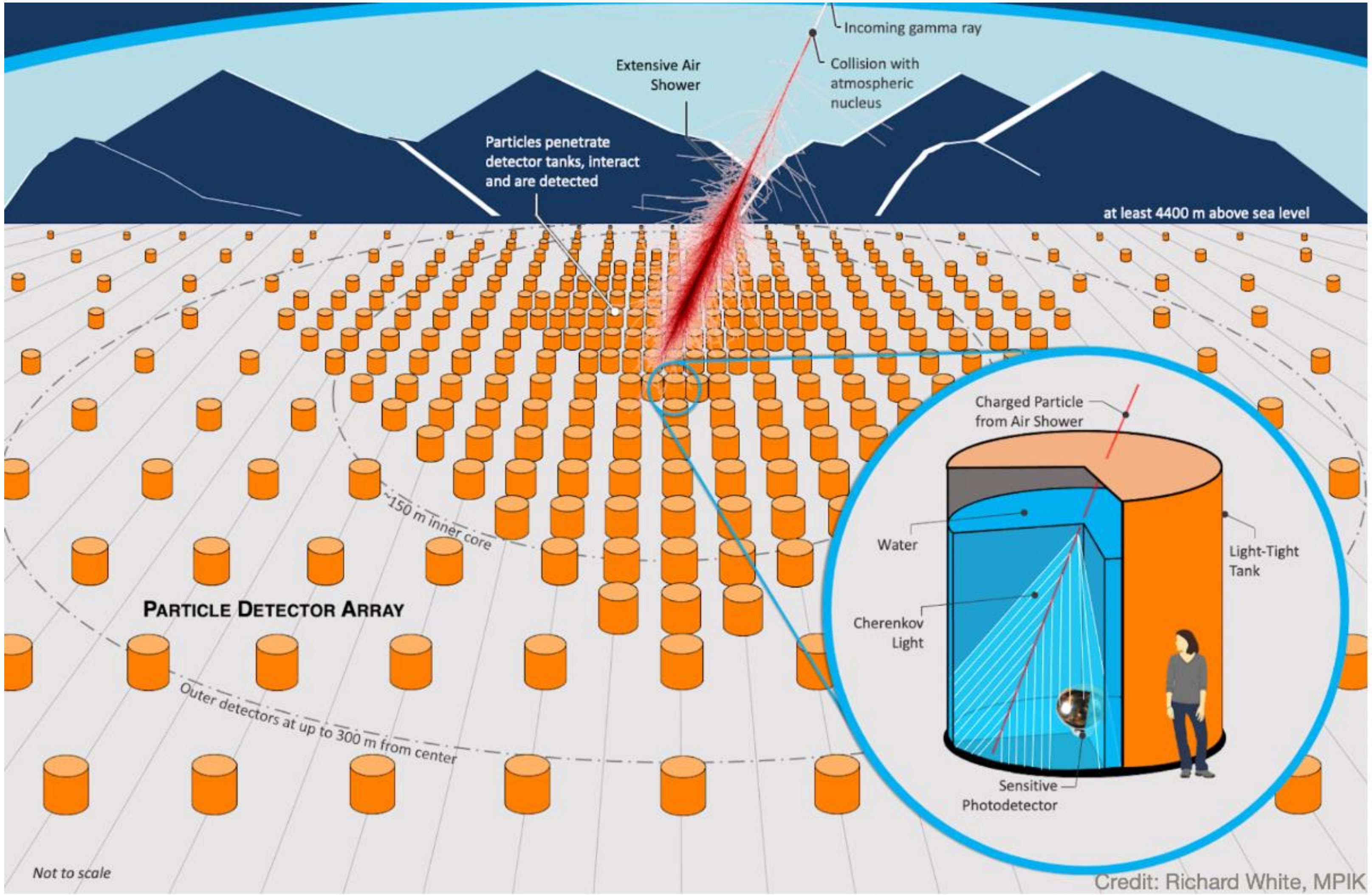
- SWGO must be at an altitude (>4.4 km) at which the shower electrons penetrate the walls of the water tanks, then generate Cerenkov light.
- Operable 24 hrs/day, as with Auger.

- CTAO can be lower, and observes the Cerenkov light generated in the atmosphere, so it can operate only at night, like optical telescopes.
- CTAO (S) at Paranal, Chile
- CTAO (N) at La Palma, Canary Isles
- SWGO in S America, site to be selected soon

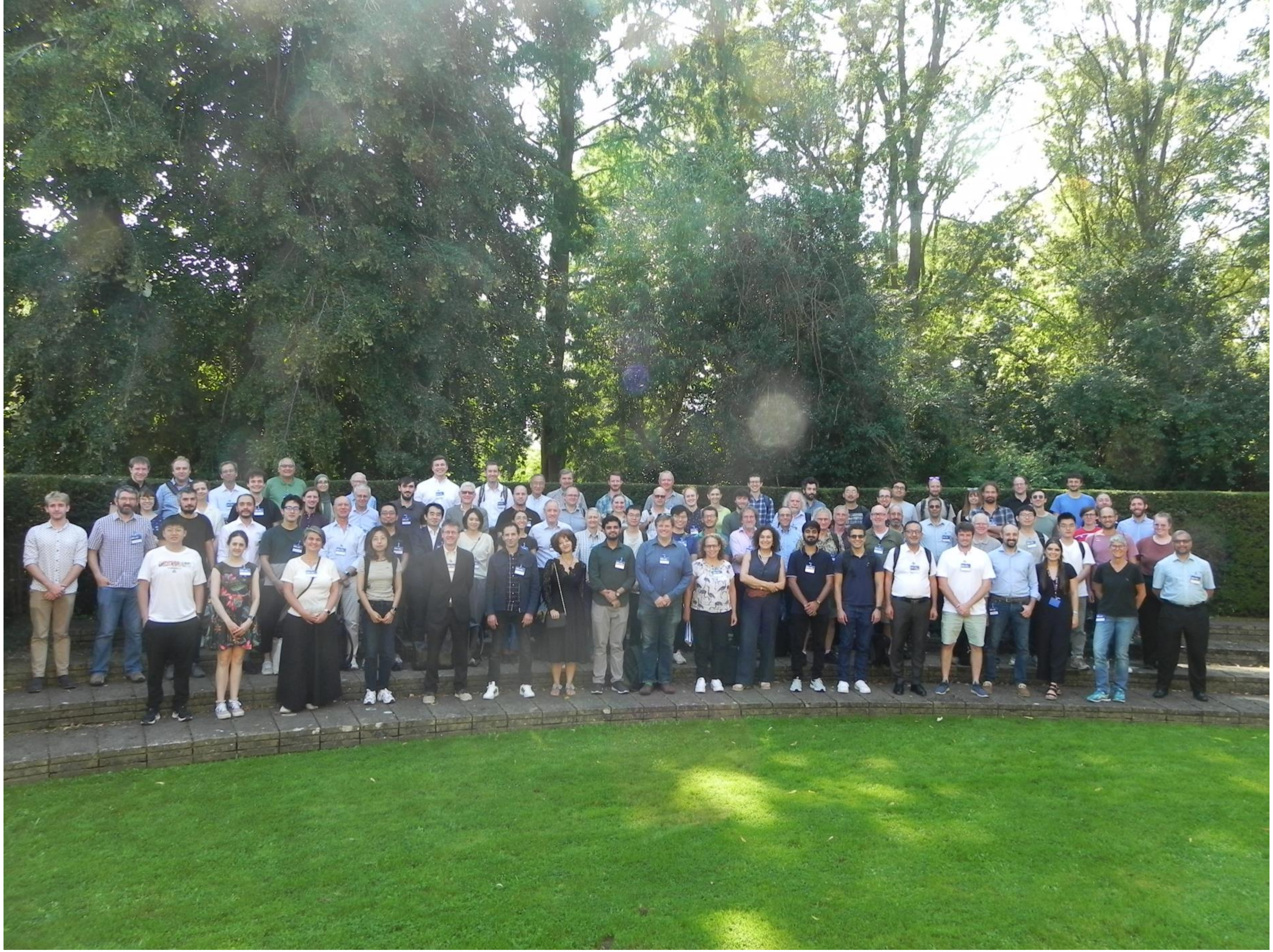
- STFC not yet convinced about UK participation



SWGO layout of water tanks

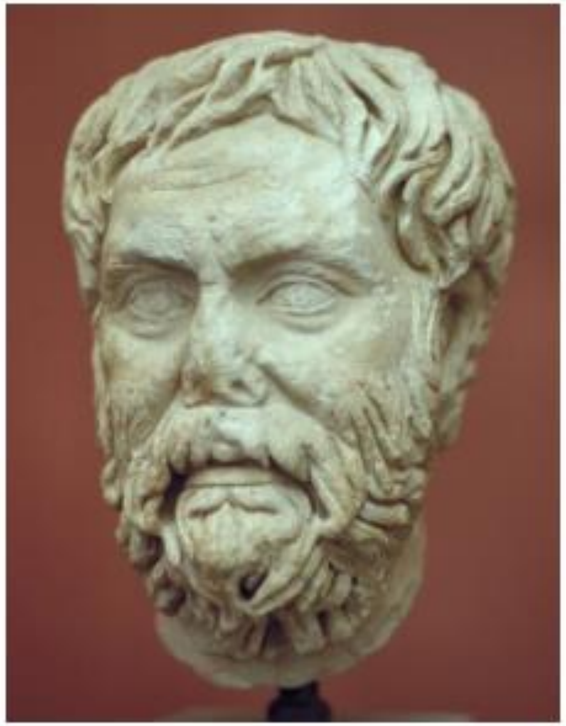


Credit: Richard White, MPIK

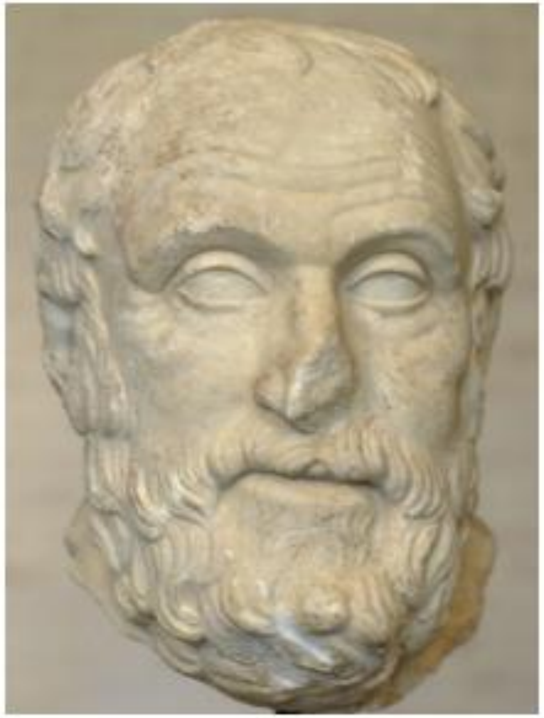


Apologies for all the wonderful work I omitted.

Subir the Skeptic



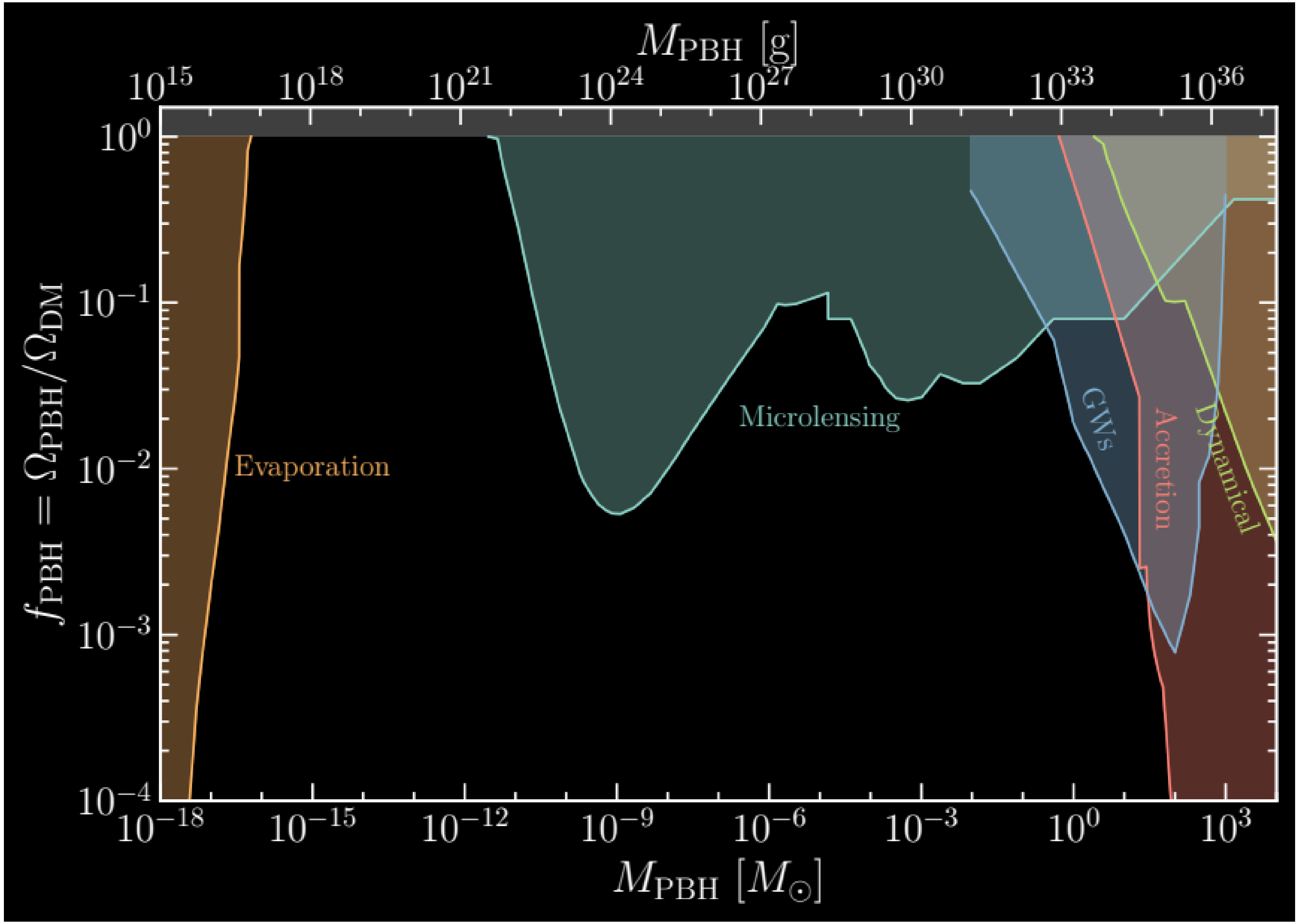
Pyrrho of Elis (360-270 BCE)



Carneades (213-128 BCE)

Subir of Oxford

Present day bounds on PBHs as DM



M(sun) = 2.0 x 10^33 g

M(earth) = 5.9 x10^27 g

M(Everest) = 1.6x10^17 g

Green and Kavanagh 2020

The Gaia Satellite

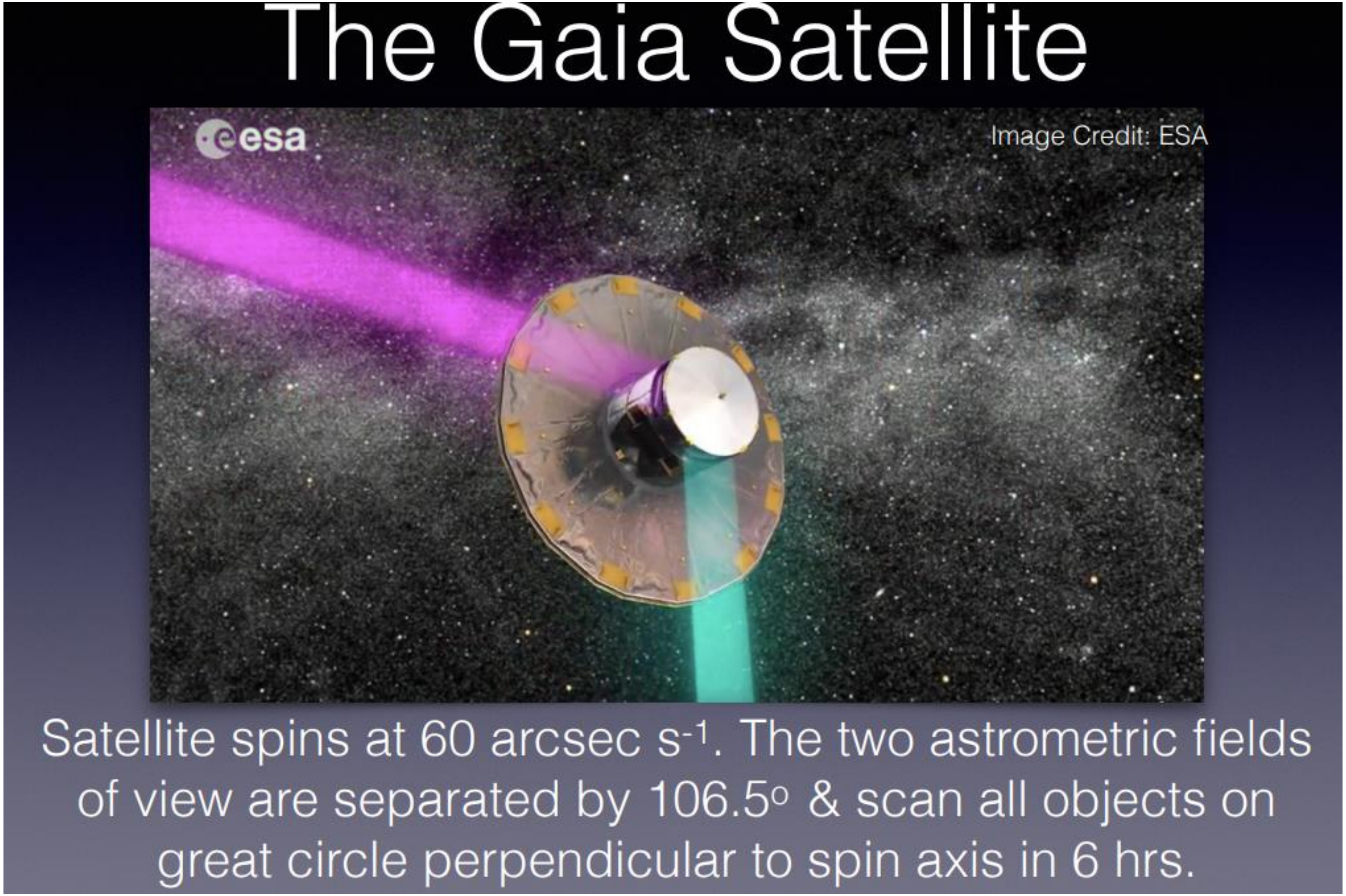


Image Credit: ESA

Satellite spins at 60 arcsec s^{-1}. The two astrometric fields of view are separated by 106.5^{o} & scan all objects on great circle perpendicular to spin axis in 6 hrs.

Largest 3D space catalogue ever, and highest angular precision

Lagrange Point L2. By parallax, determine distance and proper motion of every object

Amazing CCDs from Te2V

10^9 MW stars (mostly). Each observed 70 times over 5 years

Wide band – near UV to near IR

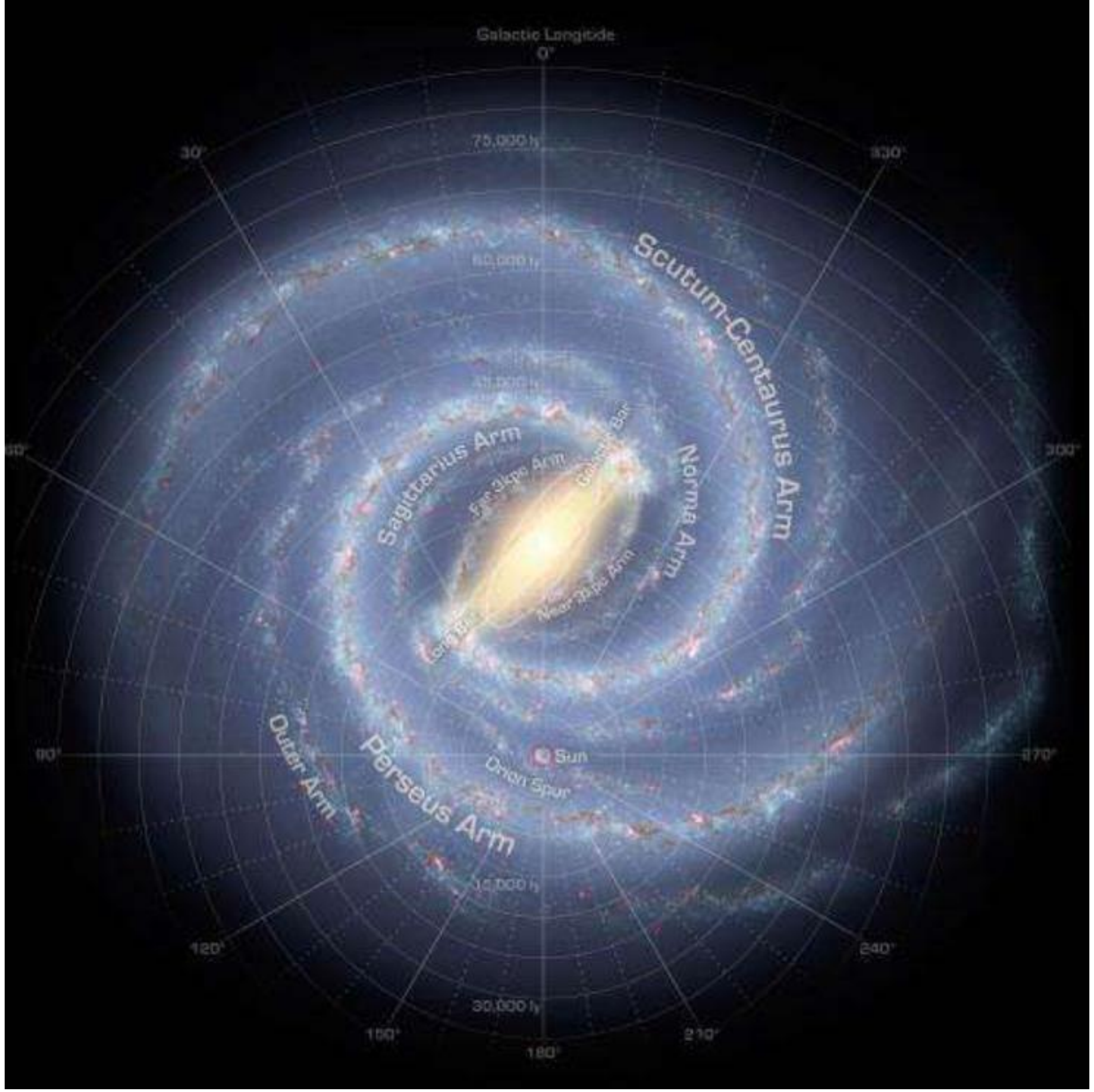
Nominally 2014-2019, but exceeding design lifetime – extended to 2025

Wyn Evans, Cambridge

Dark matter hurricanes, cyclones and downbursts

Wyn Evans, Cambridge

Has this anything to do with GAIA? No reply from Evans



Rotation period of Milky Way Galaxy is 225 million years.

Last time our Solar System was in this location,
dinosaurs were starting to arise

Subir’s punchline from his 3-day Fest:

‘It’s wonderful to have a job where every day, you can get out of bed hoping to prove that everything that went before is completely *wrong’*

Equally wonderful I think, that a variant of this can be shared by everybody – from an 11 month-old baby determined to start walking *today,* to an equally determined 92-year old patient in a care home