Liverpool main interests

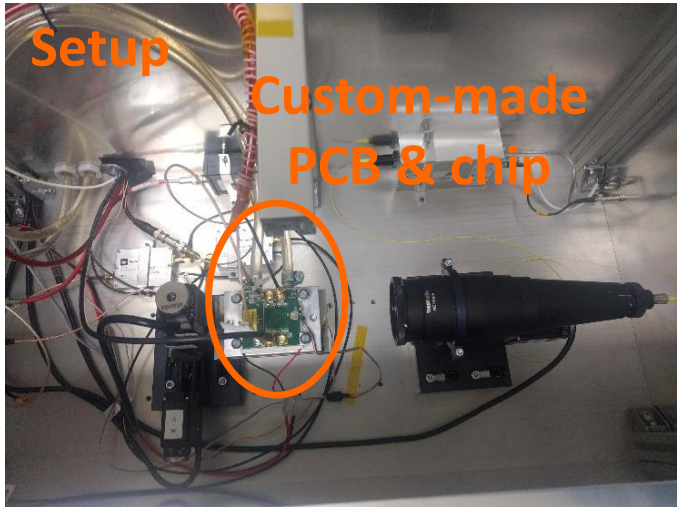
- **DRD3.1 CMOS**
  - HV-CMOS
  - Radiation tolerance
  - Speed for high rate experiments
    - Design (digital and analogue)
    - Evaluation
  - Affordable technology nodes (LFoundry)
- **DRD3.1 monolithic LGADs**
  - Pixelated and timing performance)
  - LFoundry
  - FBK
    - Industry partnership, design and evaluation
- **DRD3.1 3D interconnect**
  - Industry partnership and evaluation

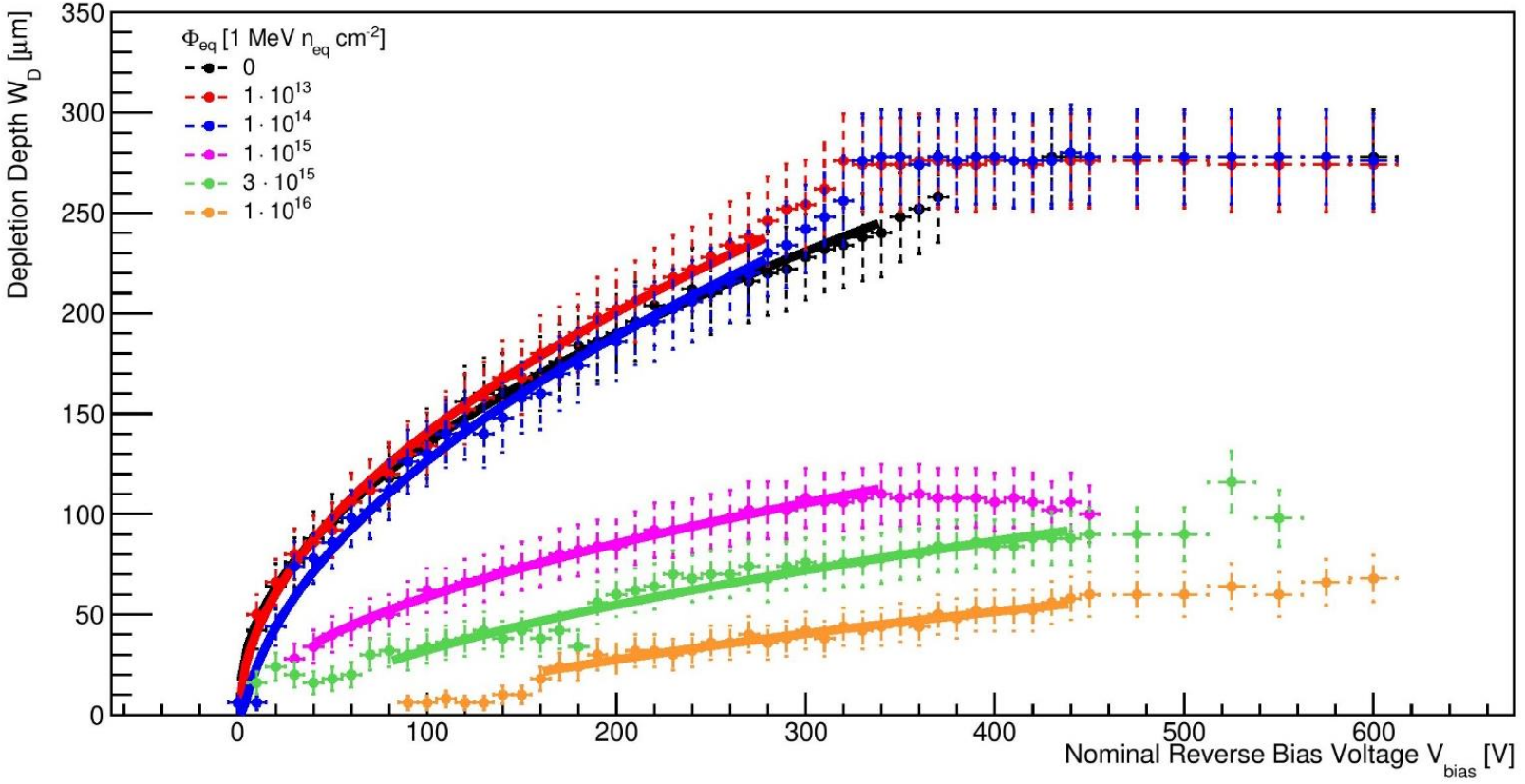
CMOS sensors (HV-CMOS) – Radiation tolerance

- **Aligned with** Research Theme 1.4 in DRD3 proposal
- **Specification value** Beyond 1E16 n_{eq}/cm^2 NIEL and 500 MRad TID
- **Strategic projects** HL-LHC (to replace innermost layers), FCC-hh
- **Research plan** TCAD simulations
  Chip design
  Evaluation of fabricated sensors including test beams
- **Deliverables** MPW submissions in cost affordable technology nodes (e.g. LF)
  MPW has test structures and small active matrices
  MPW investigates guard ring structures to achieve HV beyond 1E16 n_{eq}/cm^2
  MPW uses substrate variants, and backside biasing
  Submission 1 in Q4-2024, submission 2 in Q1-2026
- **Cost** 5 mm x 5 mm submission = 50k EUR
  5 mm x 2 cm submission = 150k EUR
  Backside biasing = 10k EUR
  Staff = 2 ASIC designers (PDRAs/Engineers), 2 PhD students

HV-CMOS radiation tolerance

Wade IWORID 2022





- Depletion voltage 300 V @ 1e14 n_{eq}/cm^2 (280 µm)
- > 50µm depleted depth @ 1e16 n_{eq}/cm^2
- Irradiated PIII + LA samples currently being evaluated