UNIVERSITY OF
BIRMINGHAM

Opportunities in sensors

L. Gonella

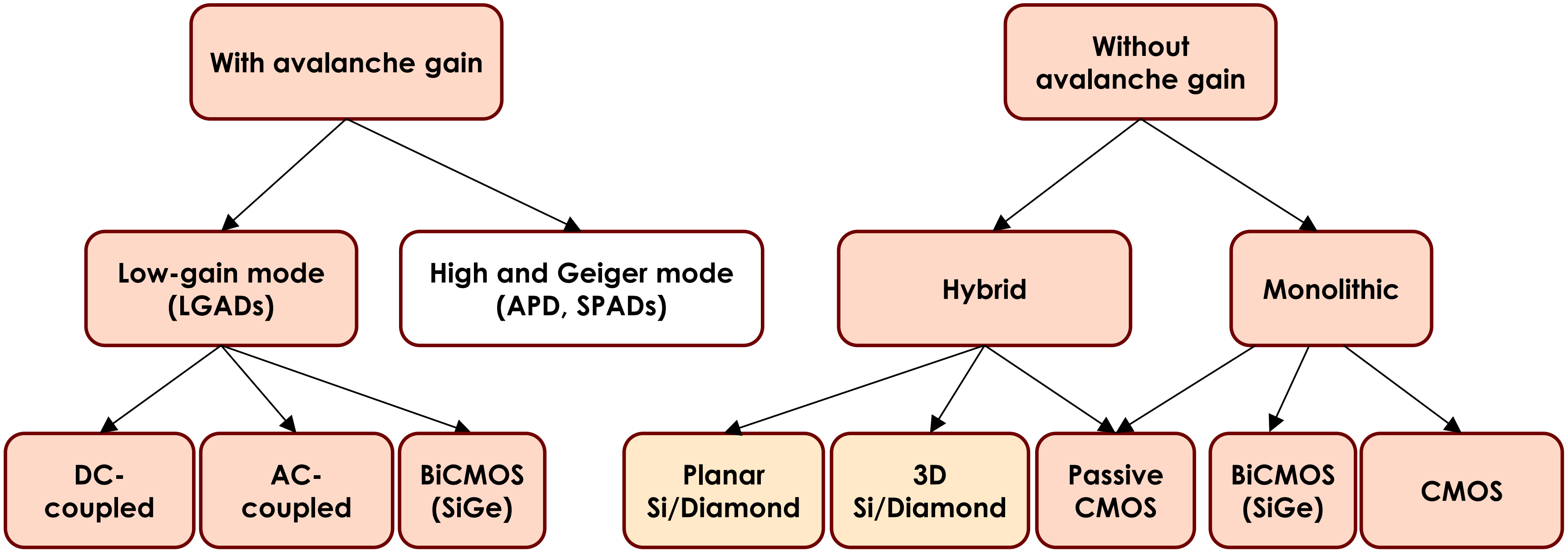
Future UK Silicon Vertex & Tracker R&D Workshop

7 – 8 September 2022

Solid state detector technologies

ECFA
European Committee for Future Accelerators

Solid state detectors for future (4D) trackers



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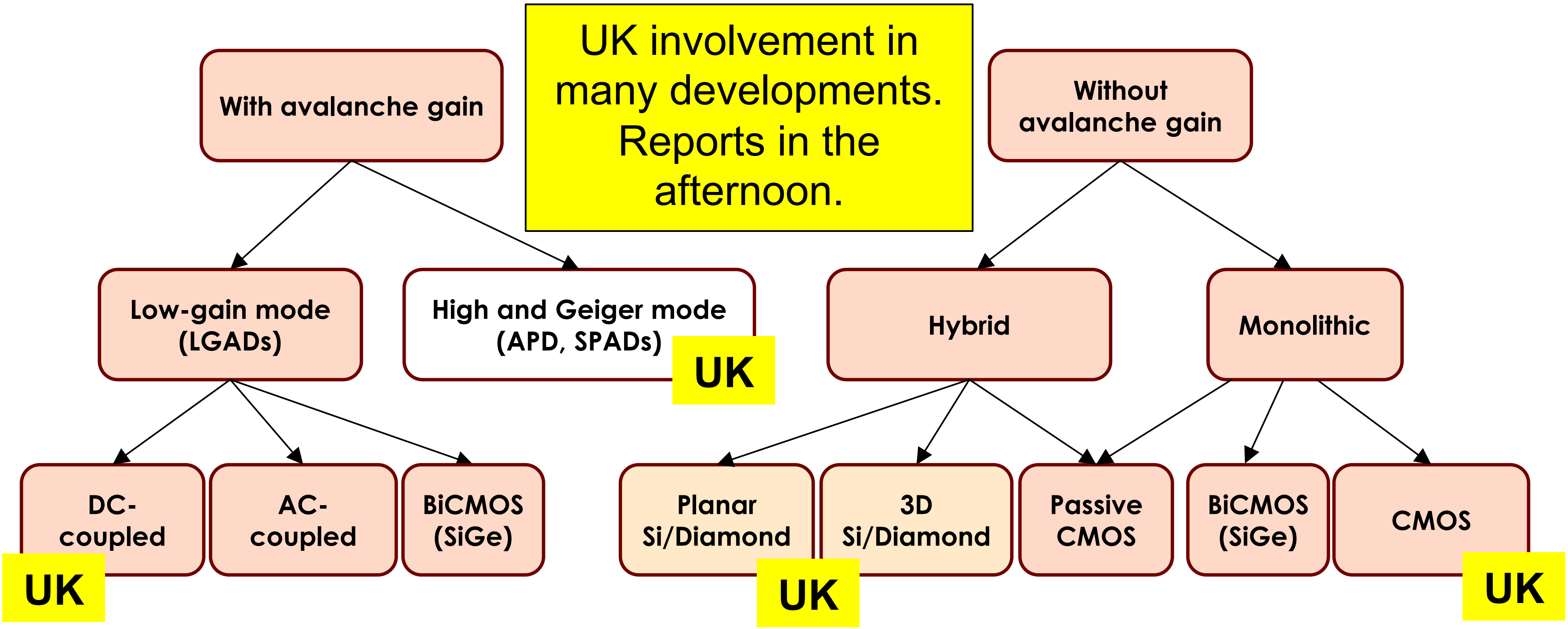
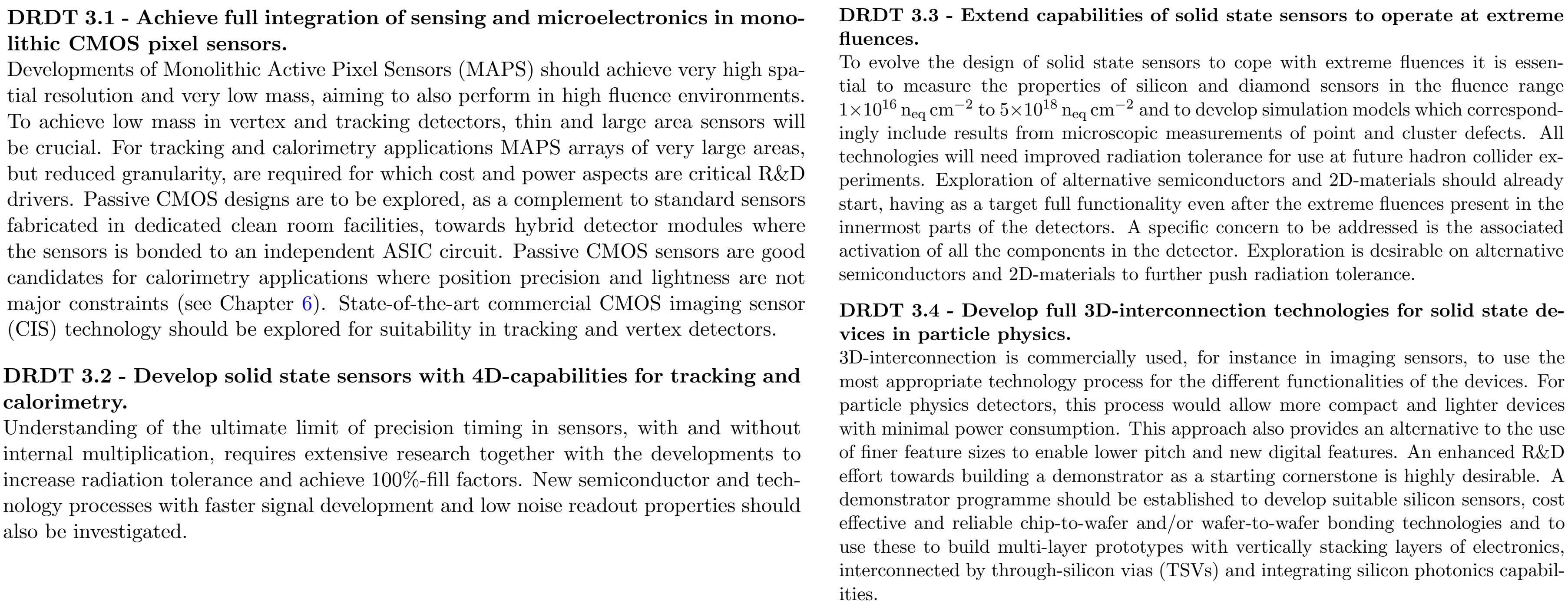


UK involvement in many developments. Reports in the afternoon.

- With avalanche gain
  - Low-gain mode (LGADs)
    - DC-coupled **UK**
    - AC-coupled
    - BiCMOS (SiGe)
  - High and Geiger mode (APD, SPADs) **UK**
- Without avalanche gain
  - Hybrid
    - Planar Si/Diamond **UK**
    - 3D Si/Diamond
    - Passive CMOS
  - Monolithic
    - Passive CMOS
    - BiCMOS (SiGe)
    - CMOS **UK**

How do we go forward?

International context - ECFA Detector R&D Themes



DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.
Developments of Monolithic Active Pixel Sensors (MAPS) should achieve very high spatial resolution and very low mass, aiming to also perform in high fluence environments. To achieve low mass in vertex and tracking detectors, thin and large area sensors will be crucial. For tracking and calorimetry applications MAPS arrays of very large areas, but reduced granularity, are required for which cost and power aspects are critical R&D drivers. Passive CMOS designs are to be explored, as a complement to standard sensors fabricated in dedicated clean room facilities, towards hybrid detector modules where the sensors is bonded to an independent ASIC circuit. Passive CMOS sensors are good candidates for calorimetry applications where position precision and lightness are not major constraints (see Chapter 6). State-of-the-art commercial CMOS imaging sensor (CIS) technology should be explored for suitability in tracking and vertex detectors.

DRDT 3.2 - Develop solid state sensors with 4D-capabilities for tracking and calorimetry.
Understanding of the ultimate limit of precision timing in sensors, with and without internal multiplication, requires extensive research together with the developments to increase radiation tolerance and achieve 100%-fill factors. New semiconductor and technology processes with faster signal development and low noise readout properties should also be investigated.

DRDT 3.3 - Extend capabilities of solid state sensors to operate at extreme fluences.
To evolve the design of solid state sensors to cope with extreme fluences it is essential to measure the properties of silicon and diamond sensors in the fluence range $1{\times}10^{16}\,\mathrm{n_{eq}\,cm^{-2}}$ to $5{\times}10^{18}\,\mathrm{n_{eq}\,cm^{-2}}$ and to develop simulation models which correspondingly include results from microscopic measurements of point and cluster defects. All technologies will need improved radiation tolerance for use at future hadron collider experiments. Exploration of alternative semiconductors and 2D-materials should already start, having as a target full functionality even after the extreme fluences present in the innermost parts of the detectors. A specific concern to be addressed is the associated activation of all the components in the detector. Exploration is desirable on alternative semiconductors and 2D-materials to further push radiation tolerance.

DRDT 3.4 - Develop full 3D-interconnection technologies for solid state devices in particle physics.
3D-interconnection is commercially used, for instance in imaging sensors, to use the most appropriate technology process for the different functionalities of the devices. For particle physics detectors, this process would allow more compact and lighter devices with minimal power consumption. This approach also provides an alternative to the use of finer feature sizes to enable lower pitch and new digital features. An enhanced R&D effort towards building a demonstrator as a starting cornerstone is highly desirable. A demonstrator programme should be established to develop suitable silicon sensors, cost effective and reliable chip-to-wafer and/or wafer-to-wafer bonding technologies and to use these to build multi-layer prototypes with vertically stacking layers of electronics, interconnected by through-silicon vias (TSVs) and integrating silicon photonics capabilities.

DRDTs provide a framework for future R&D in solid state.
Where and how do we want to participate?

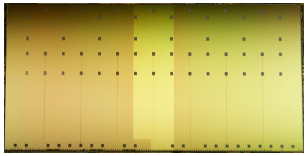
Monolithic CMOS pixel sensors

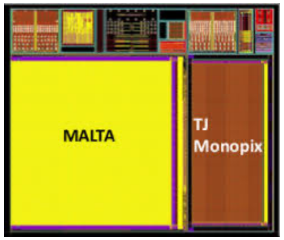
- High granularity and low power consumption demonstrated by state-of-the art (e.g. ALPIDE), further improved by the use of smaller technology nodes → vertexing at e+e- experiments.

- Large R&D programme in fully depleted MAPS the past 10 years achieved proven radiation hardness up to ~2E15 1 MeV n_{eq}/cm^2 → opens path to exploitation also in high radiation environments.

- Low cost, large volume production and ease of assembly favour use in large area trackers (i.e. CMOS is the new strips).
  - Tracking detectors is an area where there is a lot of UK expertise.
  - Also consider overlapping requirements with calorimeters, and UK work on this, possible synergies?

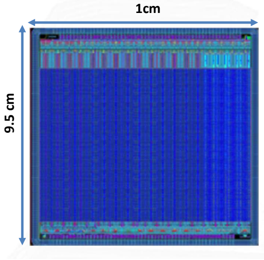
ALPIDE @ ALICE ITS

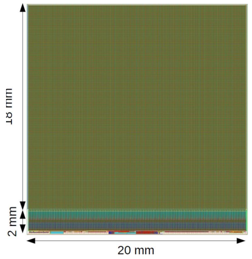




MALTA and TJ-MONOPIX
180 nm TJ

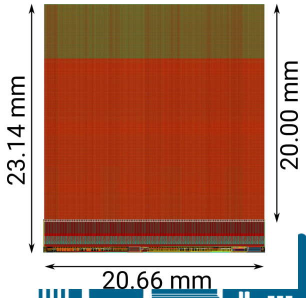
LF-MONOPIX
150 nm LFoundry





ATLASPix3
180 nm TSI

MuPix10



Monolithic CMOS pixel sensors

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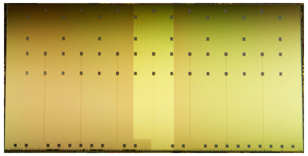
- Large R&D programme in fully depleted MAPS the past 10 years achieved proven radiation hardness up to ~2E15 1 MeV n_{eq}/cm^2 → opens path to exploitation also in high

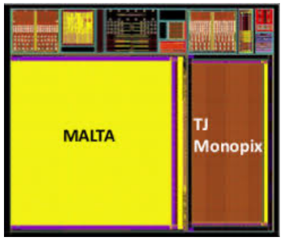
Monolithic CMOS sensor technology for HEP matured significantly in the past decade.

Upcoming experiments (Mu3e, ALICE ITS3, EIC, LHCb upgrades, ...) will consolidate its use in vertex and (large) tracking systems for the future.

  - Also consider overlapping requirements with calorimeters, and UK work on this, possible synergies?

ALPIDE @ ALICE ITS





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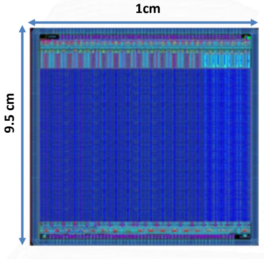

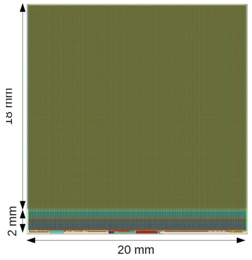

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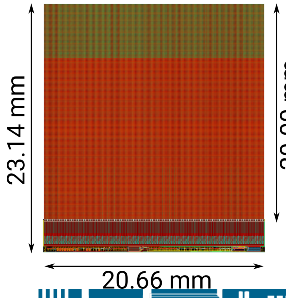


Traditional hybrid pixel detectors (not 4D)

- Technology of choice (still) for vertex detectors in high luminosity experiments.

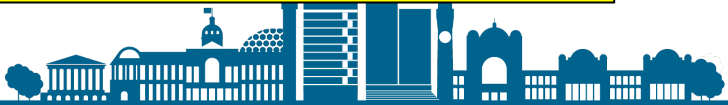
- State-of-the-art pixel detectors for HL-LHC achieve radiation-hardness up to ~1E16 1 MeV n_{eq}/cm^2 fluence and 5MGy TID, hit rate up to 3 GHz/cm^2.

- Developments for future applications target reduction of price and complexity, smaller pixel pitch, higher logic density.
  - Passive CMOS sensor (planar sensors fabricated at CMOS imaging foundries).
  - New interconnection technologies (fine pitch bump-bonding, ACF, …).
  - 65 → 28 nm ASICs.

Possibly not too attractive for future e+e-.

Currently only possibility for vertex at future hh colliders, but so far in future that other options might also become available.

Of more interest are hybrids with 4D capability.

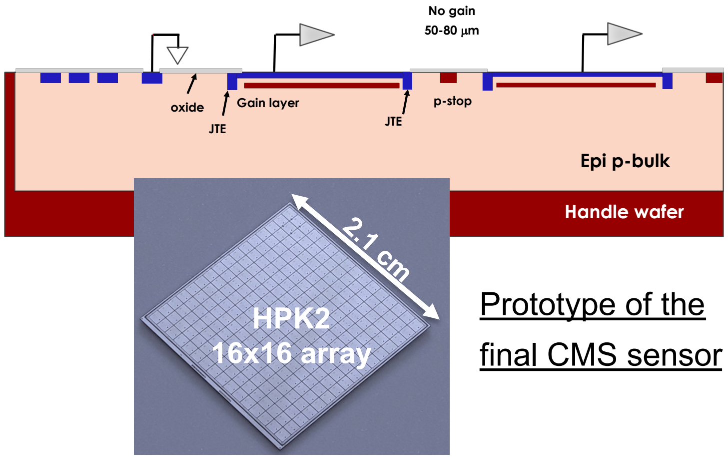


Towards 4D trackers

- State-of-the art: ATLAS & CMS timing layers.
  - 1.3 x 1.3 mm^2 pads UFSD (LGAD).
  - ALTIROC & ETIROC ASICs, 200-300 mW/cm^2.
  - Resolution ~ 45 ps/hit.

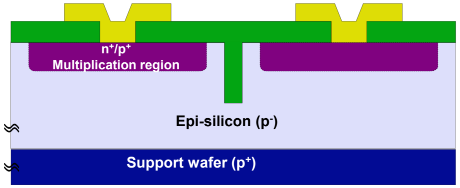
- Advanced prototypes:
  - Timepix4 soon to be coupled with TI-LGAD.
    - 55 x 55 μm^2 pixels, ~ 0.6 mW/cm^2, target resolution <100 ps/hit.
  - TIMESPOT1 with trenched (3D) detectors.
    - 55 x 55 μm^2 pixels, ~ 5-10 W/cm^2, resolution ~ 30 ps/hit.

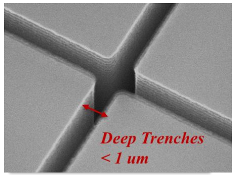
- Demonstrators:
  - Resistive readout (large pixels, excellent spatial and temporal resolution).
  - Monolithic developments: FASTPIX (CMOS), MonPicoAD (SiGe), Monolith (SiGe, w/ gain).



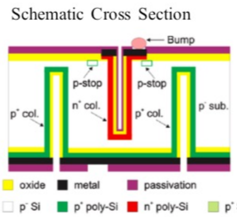
Prototype of the final CMS sensor

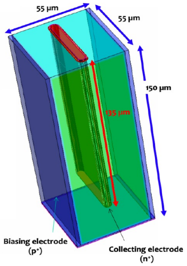
Trench Isolated LGAD

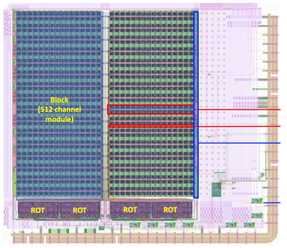




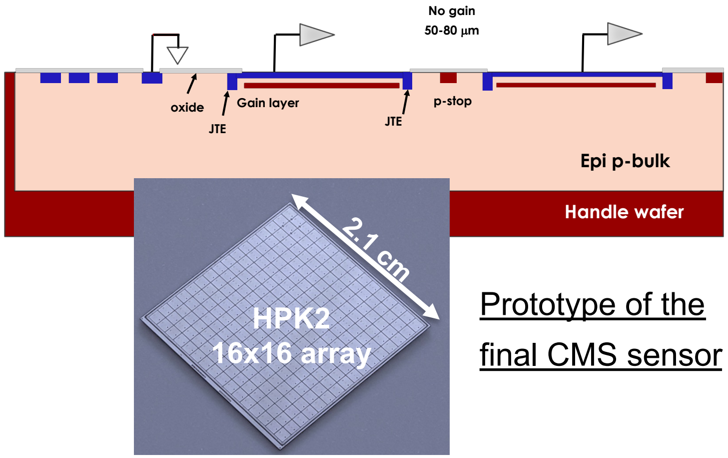
TIMESPOT







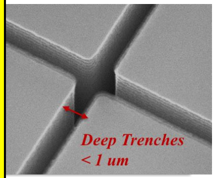
Towards 4D trackers



Prototype of the final CMS sensor

- ☐ State-of-the art: ATLAS & CMS timing layers.
  - – 1.3 x 1.3 mm^2 pads UFSD (LGAD).
  - – ALTIROC & ETIROC ASICs, 200-300 mW/cm^2.
  - – Resolution ~ 45 ps/hit.

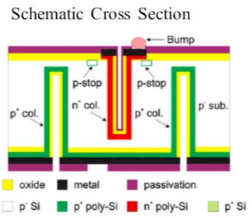
Trench Isolated LGAD

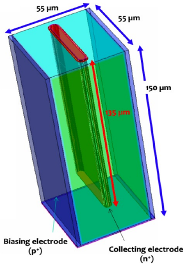


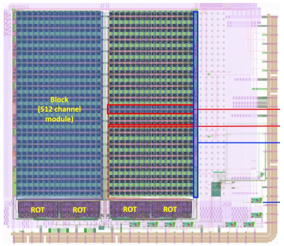
Challenges to get to 4 trackers:
spatial resolution & low power ASICs.

Latest developments include developments of monolithic 4D sensors and use of alternative technologies to silicon (SiGe).

- ☐ Advanc
  - – Ti
  - – TI
    - ☐ 55 x 55 μm^2 pixels, ~ 5-10 W/cm^2, resolution ~ 30 ps/hit.







- ☐ Demonstrators:
  - – Resistive readout (large pixels, excellent spatial and temporal resolution).
  - – Monolithic developments: FASTPIX (CMOS), MonPicoAD (SiGe), Monolith (SiGe, w/ gain).

Considerations to choose opportunities

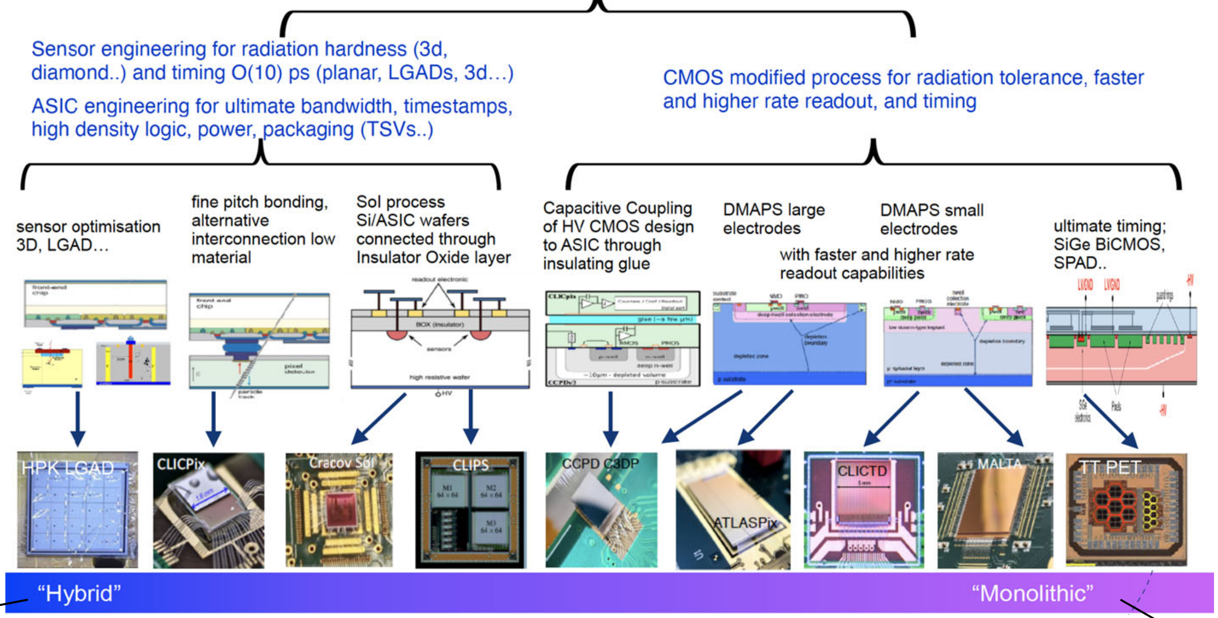
- UK expertise and interests
  - There is plenty of expertise in solid state detectors in the UK, and many different physics interests.
  - Can we converge on a few, common R&D themes that suit multiple physics tastes (i.e. colliders/experiments) and bring together all expertise?
- UK links with industry
  - Involvement of UK industry is a bonus in any proposal and participation in R&D and construction can increase UK role at future facilities.
  - Consider also links with industry overseas (e.g. RAL – TowerJazz).
- Leadership potential
  - Is there a technology on the roadmap(s) that offers opportunity for leadership?
  - Can we (UK HEP community) have the next new idea?
- Applications beyond HEP
  - Electron microscopy, X-ray cameras, synchrotrons and Free Electron Lasers, pCT, advanced clinical beam delivery instrumentation, …

Backup

Silicon detector technologies

https://doi.org/10.1140/epjp/s13360-021-02323-w

high rate, radiation hardness, timing, packaging



Sensor engineering for radiation hardness (3d, diamond..) and timing O(10) ps (planar, LGADs, 3d…)

ASIC engineering for ultimate bandwidth, timestamps, high density logic, power, packaging (TSVs..)

CMOS modified process for radiation tolerance, faster and higher rate readout, and timing

sensor optimisation 3D, LGAD…

fine pitch bonding, alternative interconnection low material

SoI process Si/ASIC wafers connected through Insulator Oxide layer

Capacitive Coupling of HV CMOS design to ASIC through insulating glue

DMAPS large electrodes

DMAPS small electrodes

with faster and higher rate readout capabilities

ultimate timing; SiGe BiCMOS, SPAD..

There are many more prototypes!!!

Hybrid pixel detectors
– Sensor optimisation (3D, LGAD, passive CMOS, …).
– 65 → 28 nm ASICs.
– New interconnection technologies (fine pitch bump-bonding, ACF, …).

SOI, 3D integration, capacitively coupled devices.

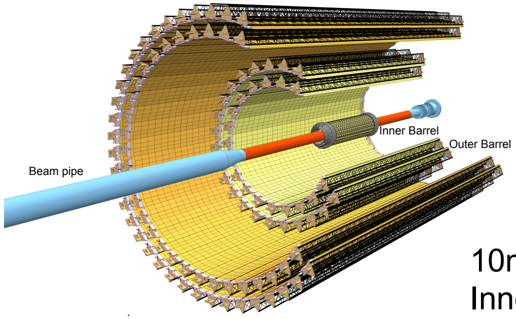
MAPS
– Improved charge collection via full depletion (HV/HR-CMOS), driven by high rate, high radiation experiments.
– Higher granularity, lower mass with smaller feature size CMOS.

SiGe BiCMOS, SPAD: Ultimate timing.

CCD (various types): Ultimate pixel size.

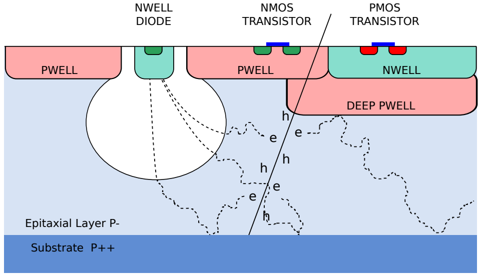
DRDT 3.1 - Monolithic CMOS

- Monolithic Active Pixel Sensors (MAPS) in commercial CMOS imaging technology could provide solutions for both vertex and tracking layers at e+e- colliders.
  - High granularity and low power consumption demonstrated by state-of-the art, further improved by the use of smaller technology nodes (see next slide).
  - Low cost, large volume production and ease of assembly would favour use in trackers wrt. strips.
    - Tracking detectors is an area where there is a lot of UK expertise.
    - Also consider overlapping requirements with calorimeters, and UK work on that → possible synergies?



ALPIDE @ ALICE ITS2
Example state-of-the-art MAPS detector

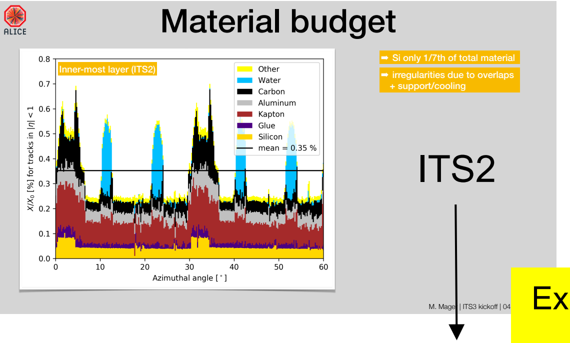
10m^2 surface
Inner Barrel = 0.3% X/X0 per layer
Outer Barrel = 0.8% X/X0 per layer
50 kHz interaction rate (Pb-Pb)
400 kHz interaction rate (pp)



180 nm CMOS TowerJazz
27 x 29 μm^2 pixel pitch
5 μs integration time
40 mW/cm^2

Stitched wafer scale sensors for cylindrical layers

- Exploration of 65 nm CMOS imaging processes for MAPS driven by CERN EP R&D WP1.2 and ALICE ITS3 upgrade.
  - 12” wafers, higher logic density, smaller pixels, faster read-out, lower power consumption.
- Wafer-scale, low power sensor design for truly cylindrical minimal material budget layers → New technology node & new detector concept.
  - Mechanical support, power distribution and data lines outside acceptance, air cooling.



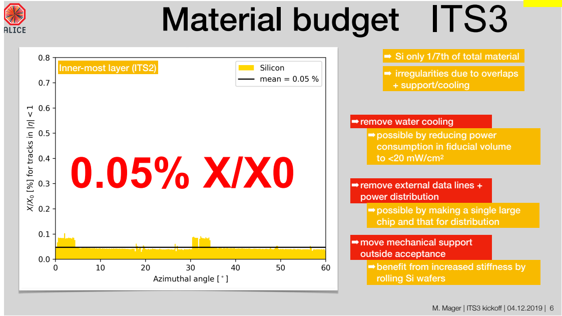
Material budget

➡ Si only 1/7th of total material

➡ irregularities due to overlaps + support/cooling

M. Mager | ITS3 kickoff | 04

ITS2



Material budget ITS3

➡ Si only 1/7th of total material

➡ irregularities due to overlaps + support/cooling

➡ remove water cooling

➡ possible by reducing power consumption in fiducial volume to <20 mW/cm²

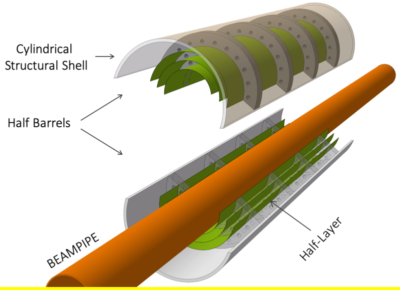
➡ remove external data lines + power distribution

➡ possible by making a single large chip and that for distribution

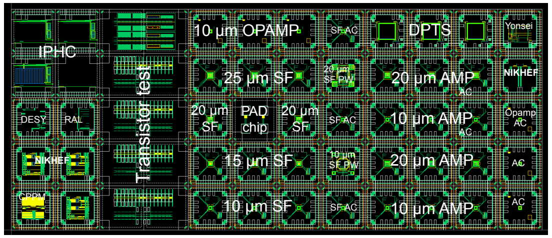
➡ move mechanical support outside acceptance

➡ benefit from increased stiffness by rolling Si wafers

M. Mager | ITS3 kickoff | 04.12.2019 | 6

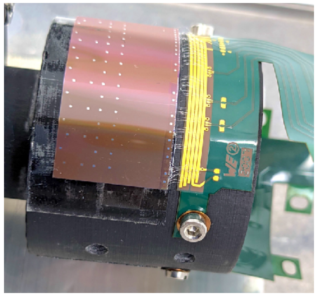


MLR1 submission

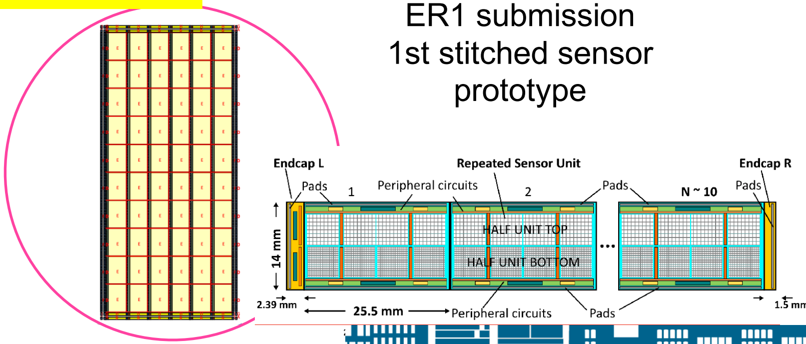


Example of emerging new technology relevant for e+e- colliders.

Bent ALPIDE

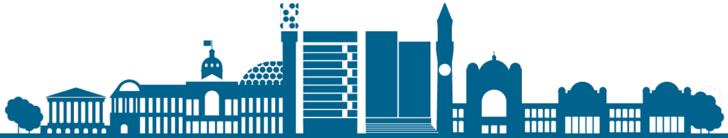


ER1 submission
1st stitched sensor prototype

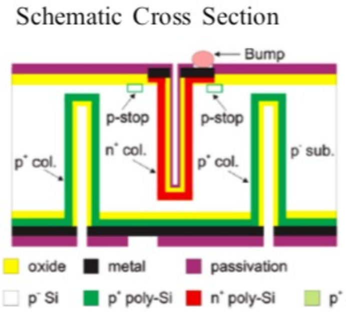


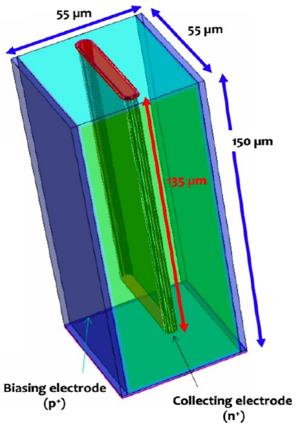
DRDT 3.4 - 3D integration

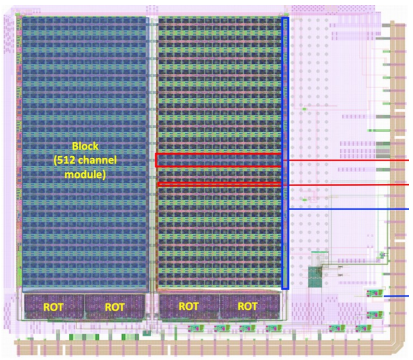
- Industrial developments of heterogeneous integration technologies to achieve further reductions in cost and power.
- 3D stacking is being studied for future HEP applications → potential for increased functionality and performance of silicon trackers.
- Pursuing this path would require large scale of investment and establishing a privileged relation with industrial partner(s), but it is a field where there isn't a clear leadership now.
  - Dependent on availability of process for R&D.
- There is expertise in the UK to work on each layer in the stack and on the interconnection technologies.



4D trackers – Hybrid, no gain







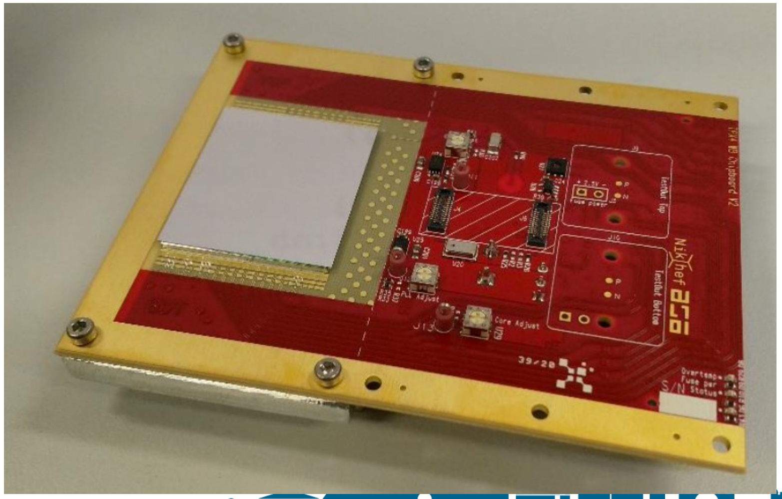
Timepix ASIC + planar sensor

Timepix4: 65 nm ASIC, 512 x 448 pixels

Pixels size = 55 um

Resolution in line with expectations ~ 150 ps RMS

Probably the best example so far of a full 4D tracking system



3D sensor + Timespot ASIC (28 nm)

Pixels size = 55 um

Resolution ~ 30 ps for single channel

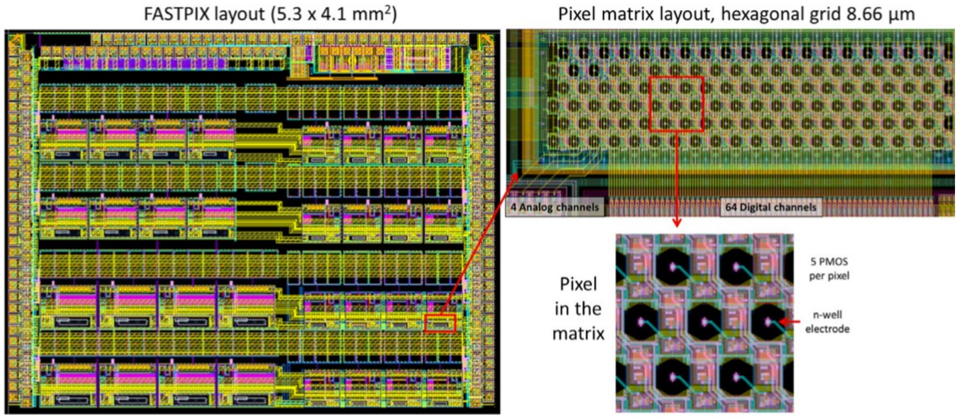
4D trackers – Monolithic, no gain

FASTPIX

temporal stamping with excellent position precision

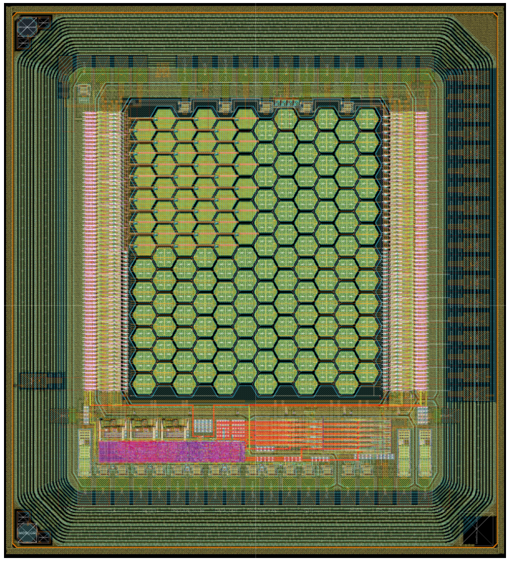
Resolution of about ~ 100 ps

Very small pixels (< 9 um)



FASTPIX layout (5.3 x 4.1 mm^2)

Pixel matrix layout, hexagonal grid 8.66 µm



MonPicoAD project

Exploit SiGe performances

Exagonal pads, 65 um

About 25 um depletion

Thinned to 60 um

Resolution of about ~ 38 ps,

Very small pixels