Opportunities in TDAQ

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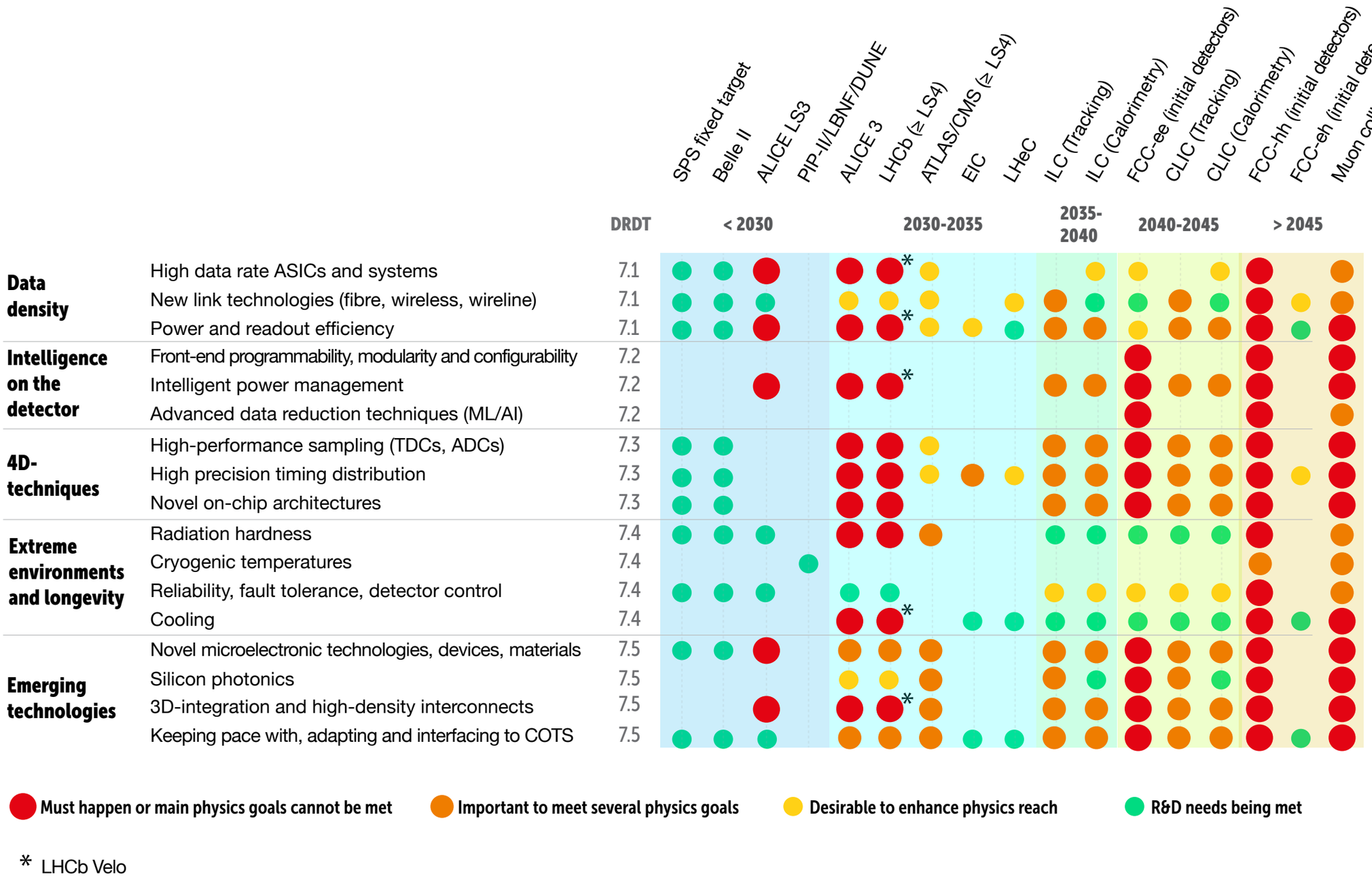
Opportunities in TDAQ

- The exciting opportunities in this area:
  - Being complex, expensive, and mission-critical
  - Being the first thing in the project to start and the last thing to work
  - Coping with everyone else's random design decisions and changes
  - Only being noticed when the system is broken
- But seriously… there are things to do in 'the back office'
  - DAQ is probably *not* a technical or cost driver for e+e- machines
    - But will be major hassle if not planned correctly from the start – witness issues in current upgrade projects
  - DAQ probably is *the* technical and cost driver for hh ($\mu\mu$?) experiments
  - Clear signs that our current approaches will need to change
    - Probably no need for complex pipelined trigger systems
    - Possibly no access to the most advanced technology nodes
    - Strong need to converge to commercial / industrial norms (and to stay current)
- Q: how can the long-term R&D programme benefit our nearer-term projects?
- My definition of DAQ is, all hardware and software involved in:
  - Data selection and movement from front-end devices to off-detector processing and storage
  - Control, configuration, synchronisation and monitoring systems for the detector electronics
  - Real-time or batch computing in the data pipeline before bulk storage
  - NOT analogue / service parts of front-end ASIC (so detector-DAQ boundary is inside the chip)

The Detector Roadmap Sayeth…



- A lot of this is about capability, expertise and industry engagement
  - Marcus and Mark have covered a lot of the ‘how’, let’s talk about ‘what’

Relevance to Future Silicon Projects

- 4D developments
  - Need for precise frequency and phase alignment – how far can we go?
  - Substantially increased data volume per hit
  - Requirement / opportunity for local data filtering
- Standardised control and readout – we need *one* each of:
  - 'Slow control' plane (redundant, reliable, simple)
  - Readout L1 protocol (perhaps over multiple physical media)
    - And it had better look like ethernet and use industry-standard data rates
  - Set of verified and exhaustively tested IP blocks to implement this
    - Implementable in either FPGAs or hardened ASICs
- Optimal use of bandwidth
  - Sparse events imply intelligent buffering for optimal readout utilisation
    - Readout could easily dominate power requirements in some subdetectors
    - Any properly optimised system will require back pressure all the way to the front end
  - Selective / regional / staged / OOO readout may have benefits
    - Implies a more complex handshake between central DAQ and front-end devices
- These statements are all 'trackerish'
  - Issues facing calorimetry are if anything more severe, may need different approaches

Other Cool Stuff for Context

- Possibly not for e+e-, but on the list
  - Timing self-calibration
  - On-chip data reduction and programmable intelligence (ML?)
  - Advanced low-power link technologies
    - Photonic, high-bandwidth galvanic, RF
  - On-detector network (local event building)
  - Smart power management (scalable bandwidth / processing)
  - Novel powering (RF)
- Also many non-collider topics to address
  - Particularly: cryogenic and deep cryogenic electronics
- Setup of an 'Electronics DRD collaboration' now under way
  - Initial discussions between major labs on support and access aspects
  - Expect to re-start community workshops in early 2023?
  - Focussed UK approach is surely needed to underwrite continued leadership
    - There are opportunities (and I hope funding) for those who wish to step up for this

Development Approach

- I argue: we need a standardised DAQ approach from the start
  - Recent history of overly complex design with some development failures
    - Approximately 40 different readout ASICs for LHC upgrades; many of them work
    - 'DAQ as a second thought' has now caused major issues in a number of projects
  - Standardised approach allows early 'realistic' testing and early development of common control systems (incl. complex real-time software)
  - Upfront development of common robust solutions (well before final design) pays off later
- How to approach this?
  - Develop and **model** data pipeline early, rather than focus on sensor / ASIC performance
    - This includes local processing at the front end, but back-end (e.g. trigger) requirements on the front end
  - Target end-to-end demonstrators, minimally ad hoc
  - Consider the 'systems issues' (power, material, space) upfront
- What should the UK do now?
  - Include strong support for 'near term' projects in the overall electronics R&D plan
  - Look again at lessons from LHC (including realistic services estimates)
  - Consider the new capabilities offered by 4D
  - Take leadership in specifying and testing common DAQ interfaces
  - Address modular design issues in and long-term IP reuse across ASIC developments
  - Embed this approach in our tracking and calorimetry prototypes