UNIVERSITY OF BIRMINGHAM

Development of 65 nm MAPS in the UK

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on behalf of Birmingham, Brunel, Lancaster, Liverpool, STFC-DL, STFC-RAL

Future UK Silicon Vertex & Tracker R&D Workshop, 7 – 8 September 2022

Motivations for 65 nm in HEP

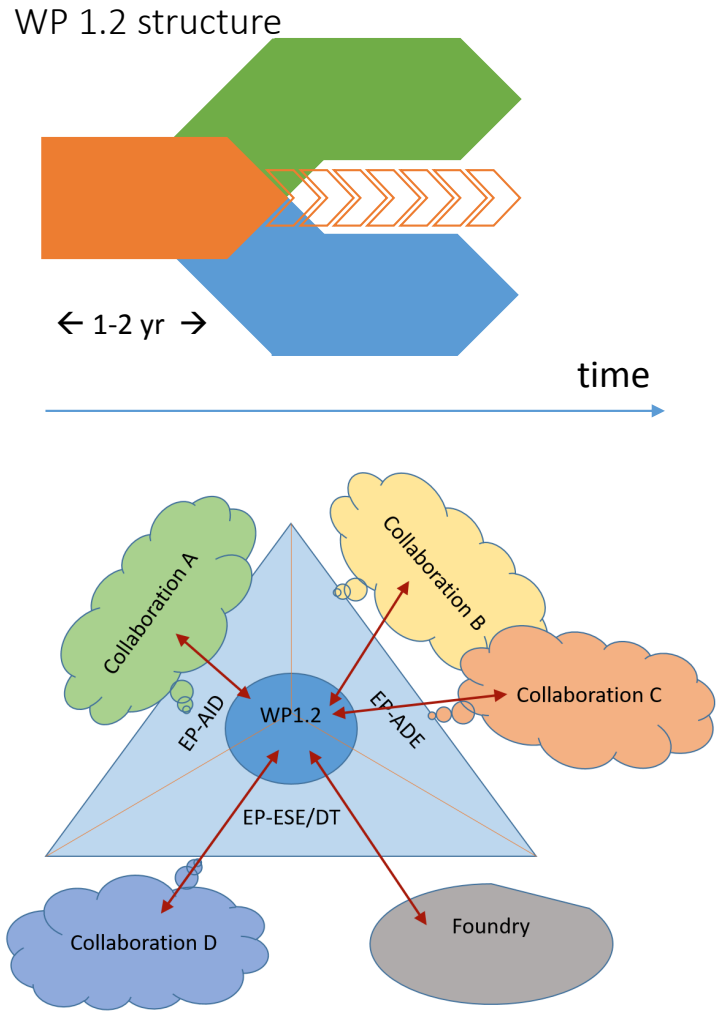
- State-of-the-art and advanced prototype MAPS for HEP use 110 - 180 nm CMOS imaging technologies (beyond mature in industry).

- Proposed future HEP facilities, planned over the next few decades will need improved performance in terms of granularity, power consumption, rate and radiation hardness → smaller feature size technology needed.

- The HEP community is starting exploration of 65 nm technologies
  - Higher logic density (increased performance/area, higher granularity)
  - Lower power
  - Higher speed (logic, data transmission…)
  - Process availability
  - Higher NRE costs and complexity, but lower price per area

CERN EP R&D programme: WP1.2 MAPS

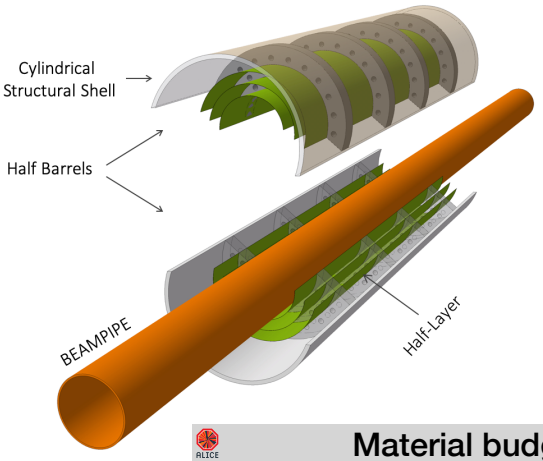
- Phase 1:
  - Initial selection and validation of a new technology (65 nm) and asynchronous architecture study (MALTA) in 180 nm.
- Phase 2:
  - Pre-prototyping of a large, low-power and high-resolution sensor ''Sensor A'' (ALICE ITS-3, future e+e-).
  - Pre-prototyping of a fast and rad hard sensor ''Sensor B/C'' (high luminosity pp experiments).
  - Continuation of common activity: Technology monitoring and survey, training, design and measurement framework.
  - Other explorations (Sensor D, …) depending on findings.



https://cds.cern.ch/record/2644611
https://doi.org/10.1016/j.nima.2021.166280
https://indico.cern.ch/event/1071914/

First application: ALICE ITS3 detector

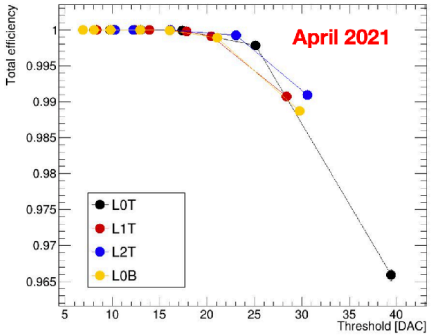
- New generation MAPS sensor at the 65 nm node to design a truly cylindrical, extremely low mass (0.05% x/X0) vertex detector for the HL-LHC Run 4.
  - Exploit stitching over large area to design wafer scale sensors.
  - Thin sensors bent around the beam pipe.
  - Lower power in 65 nm allows air cooling.
  - Minimal support needed and services outside active area.



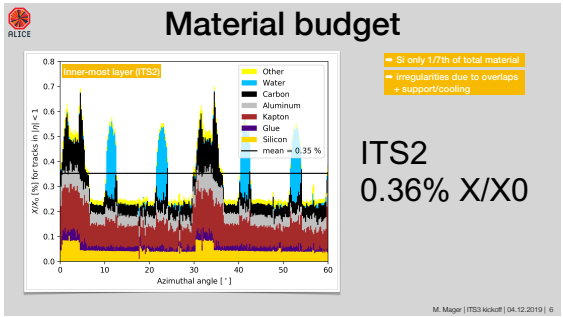
Specifications

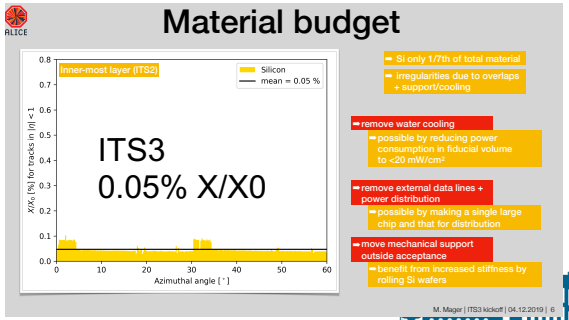
Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

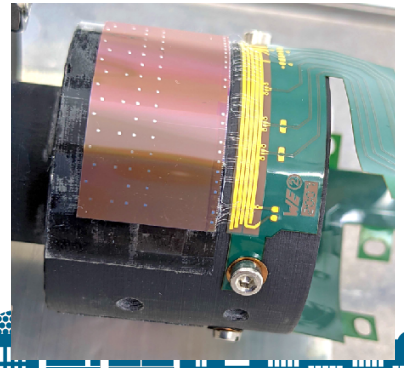
M. Mager | ITS3 kickoff | 04.12.2019



Efficiency versus bending radii with bent ALPIDE (test beam data)

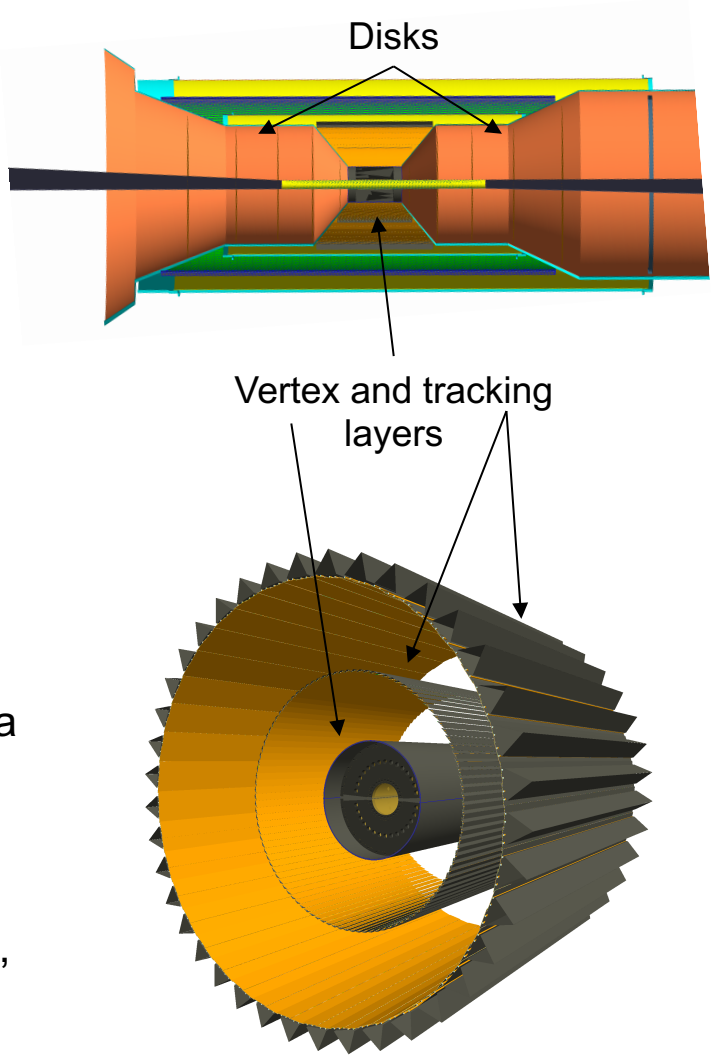






Spin-off: EIC Si Vertex and Tracking Detector

- EIC EPIC SVT detector concept derived from the ALICE ITS3 technology.
- EPIC vertex layers: ITS3 like.
  - ITS3 wafer-scale stitched sensor, thinned and bent around beam pipe.
  - No services in active area, air cooling, minimal support structure → 0.05% X/X0.
- EPIC tracking layers and disks.
  - EIC Large Area Sensor (LAS), i.e. ITS3 sensor size optimised for high yield, low cost, large area coverage.
  - Convectional carbon fibre support structures with integrated cooling.
  - Material budget estimates: 0.24% X/X0 per disk, 0.25 - 0.55% X/X0 per barrel layer



UK work on 65 nm

- Carried out in the context of the Electron-Ion Collider where there is already significant UK participation (more details in backup slides) .

- R&D funding from UKRI Infrastructure Bid, preliminary phase 2021 – 2024.
  - WP1 MAPS, WP2 TimePix (Glasgow), WP3 Polarimetry (York).

- WP1 MAPS
  - Institutes involved: Birmingham, Brunel, Lancaster, Liverpool, STFC-DL, STFC-RAL.
  - Work is carried out within the EIC Silicon Consortium and EIC project and in collaboration with ALICE ITS3 and the CERN EP R&D programme.

- WP1 tasks
  - WP1.1 – Sensor design
  - WP1.2 – Sensor characterisation and DAQ
  - WP1.3 – Modules and system tests
  - WP1.4 – Detector layout simulations

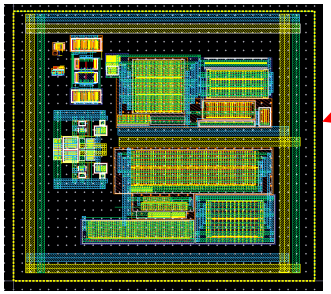
MLR1 - 65 nm prototypes

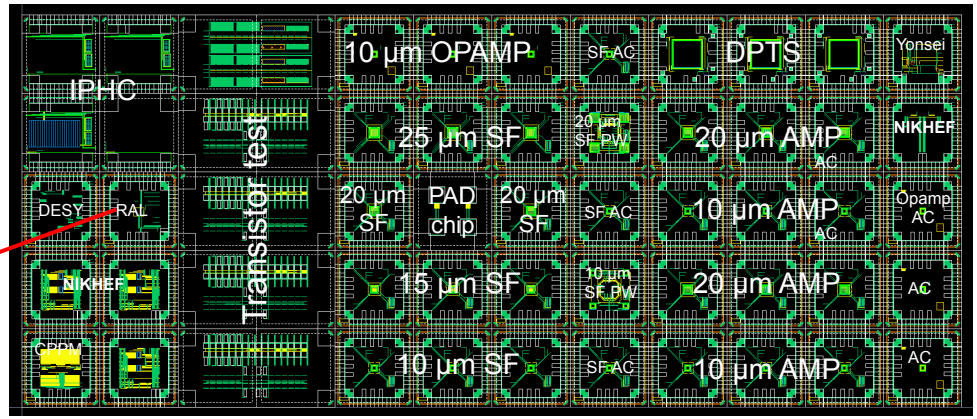
- First submission in TowerJazz 65nm as part of the CERN EP R&D WP1.2.
  - Significant drive from ITS3, important contributions from many groups.
  - Submission in Q4-2020, testing ongoing.

- Scope: Technology exploration and prototype circuit blocks for future sensors.

- Structures:
  - Analogue and Digital Pixel Test Structures (IPHC, DESY, CERN)
  - Transistor Test Structures (CERN)
  - Bandgap/VCO (NIKHEF)
  - High Speed Structures (RAL)
  - Ring Oscillator (CPPM)

RAL circuit:
LVDS receiver and CML transmitter



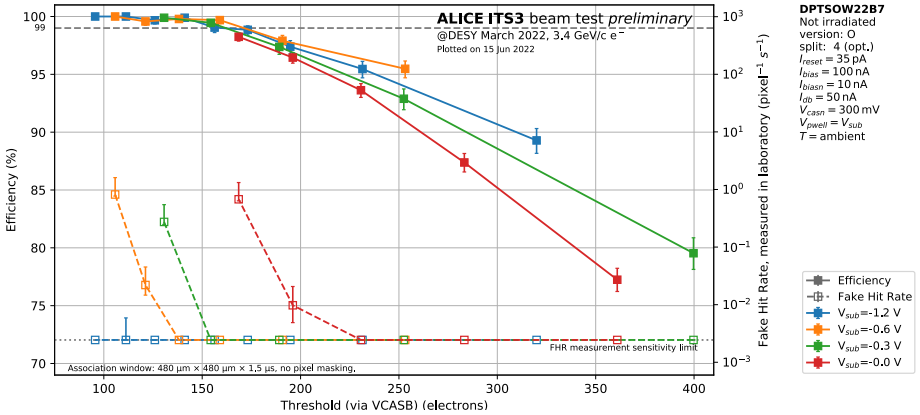


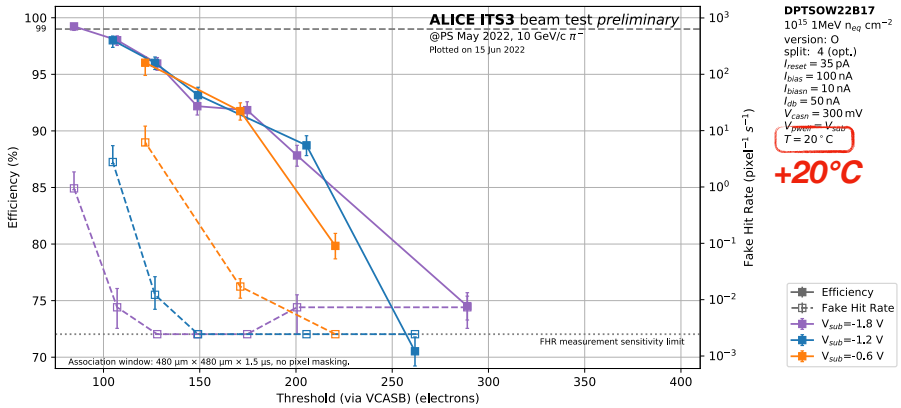
MLR1 testing and results

- Pixel test structures (APTS, DPTS, CE65) characterisation is carried out by a large number of institutes and people around ITS3.
  - More to join following ongoing distribution of readout systems and chips.

- MLR1 chips are performing exceptionally well.
  - Radiation hardness of beyond 1x10^{15} 1 MeV n_{eq}/cm^2 NIEL is attained.

DPTS beam test results: efficiency and fake hit rate



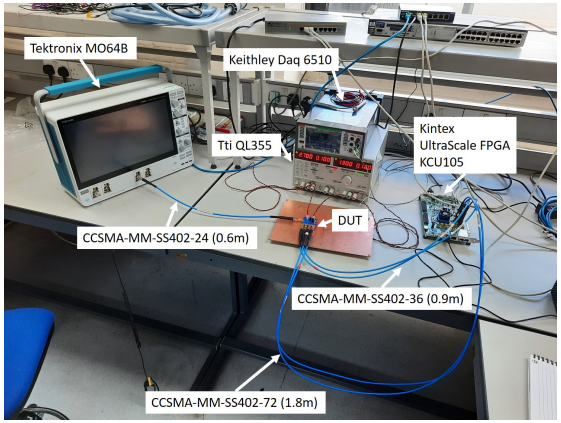


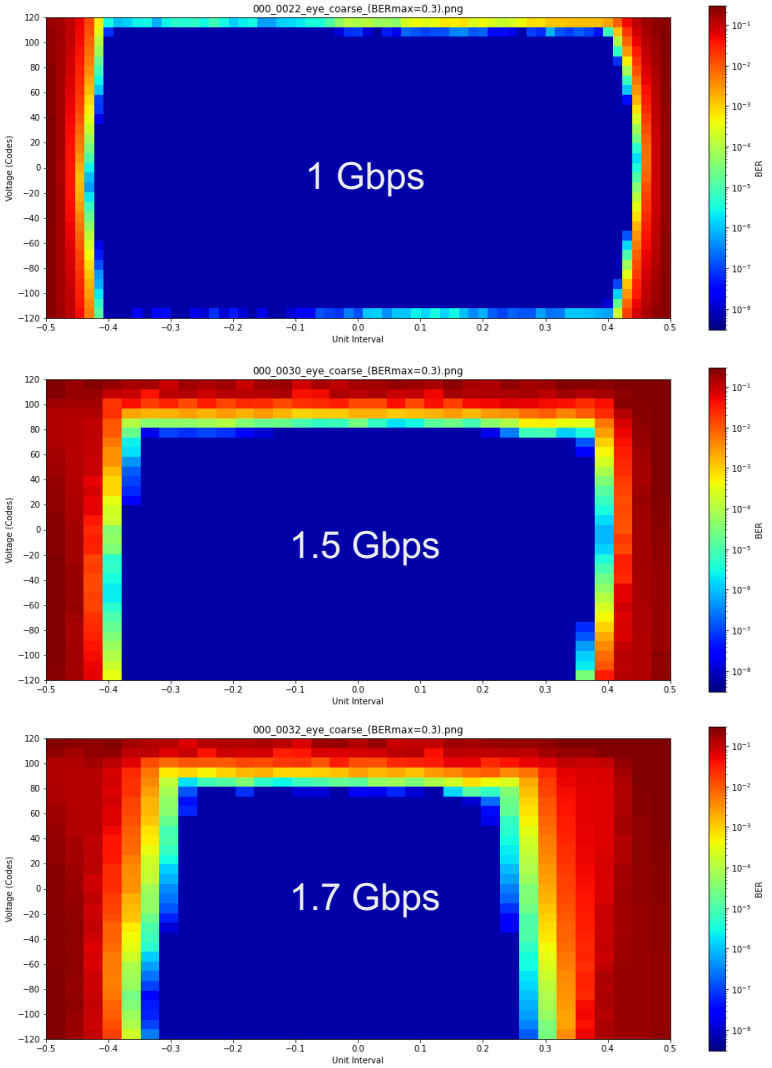
- Circuit blocks tests carried out by designing institutes.

https://indico.cern.ch/event/1156197/contributions/4855158/subcontributions/385644/attachments/2465185/4227238/2022-06-20_ERPD-ITS3.pdf

MLR1 testing in the UK

- Testing of RAL circuit block.
  - DL/RAL TD developed testing setup.
  - Chips bonded at BHM/LIV.
  - Circuit works up ~1.5 Gbps.
  - X-rays irradiations at CERN this week.



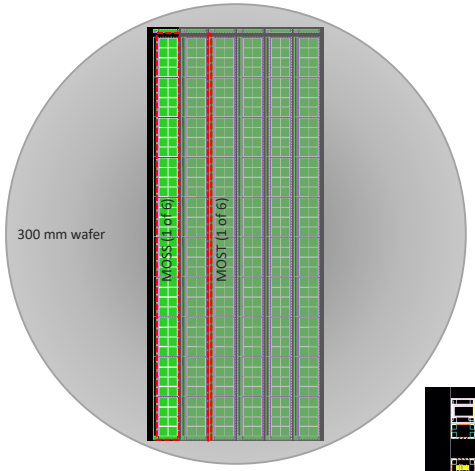


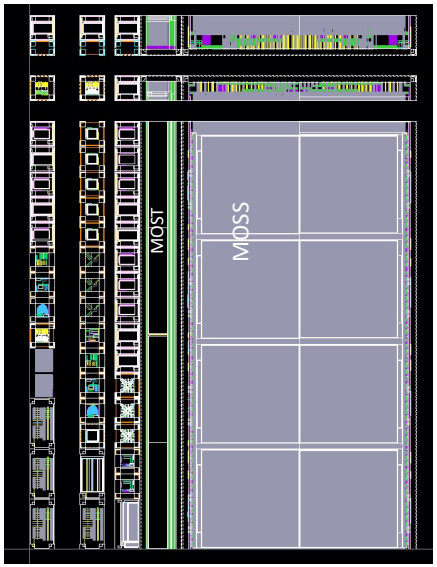
- Contribution to APTS and DPTS testing.
  - Birmingham and Liverpool are bonding sites for APTS chips.
  - Readout systems just received in Birmingham and Liverpool, more to arrive at Daresbury, Lancaster, RAL.

ER1

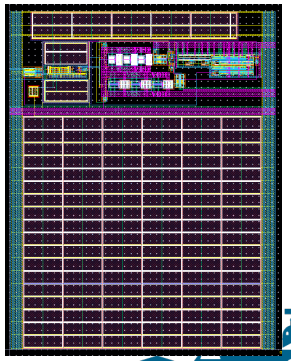
- First Engineering Run, ER1, in preparation aimed at learning about stitching and yield of large area sensor.
  - Two large stitched sensor chips: MOSS, MOST.
  - Small test and development chips.

- RAL contributions
  - PLL and CML receiver; the PLL will be integrated with the MLR1 IP blocks.
  - I2C block; of interest to the ITS3 large area sensor development for on-chip signal transmission.
  - DFM cells improvements required by the collaboration also carried out by RAL TD.

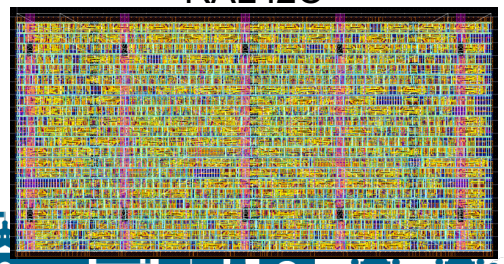




RAL PLL



RAL I2C



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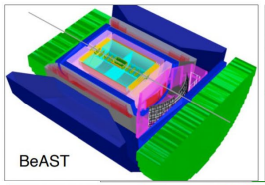
Conclusion

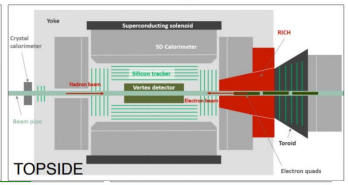
- MAPS in 65 nm CMOS imaging technology are being explored at international level through CERN EP R&D programme (5-years).
- Technology performance for application as charged particle sensors confirmed by ongoing characterisation of first test structures.
- First applications: ALICE ITS3 and EIC (linked development).
- Clear potential for vertex and tracking at future colliders.
- UK institutes are participating in the development (CERN EP R&D programme and ALICE ITS3) thanks to UKRI Infrastructure Funds for EIC.

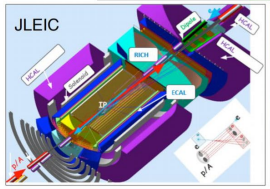
Backup

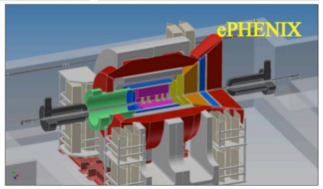
EIC Detector Concepts

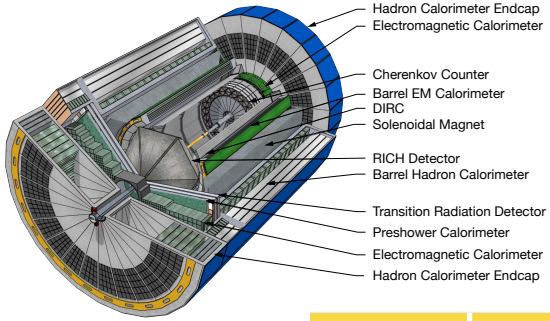
White paper (2012, 2014), initial concepts











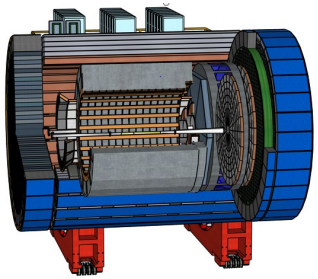
Yellow Report reference detector (2020), global effort of the EIC Users Group

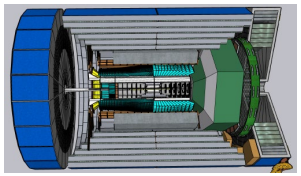
Call for Detector proposals (2021)

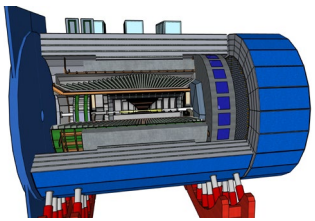
ATHENA: A Totally Hermetic Electron-Nucleus Apparatus
- General purpose detector inspired by YR studies, new central magnet of up to 3T

CORE: COmpact detectoR for the Eic
- Nearly hermetic, general purpose compact detector, 2T baseline

ECCE: EIC Comprehensive Chromodynamics Experiment
- General purpose detector, 1.5T BaBar magnet





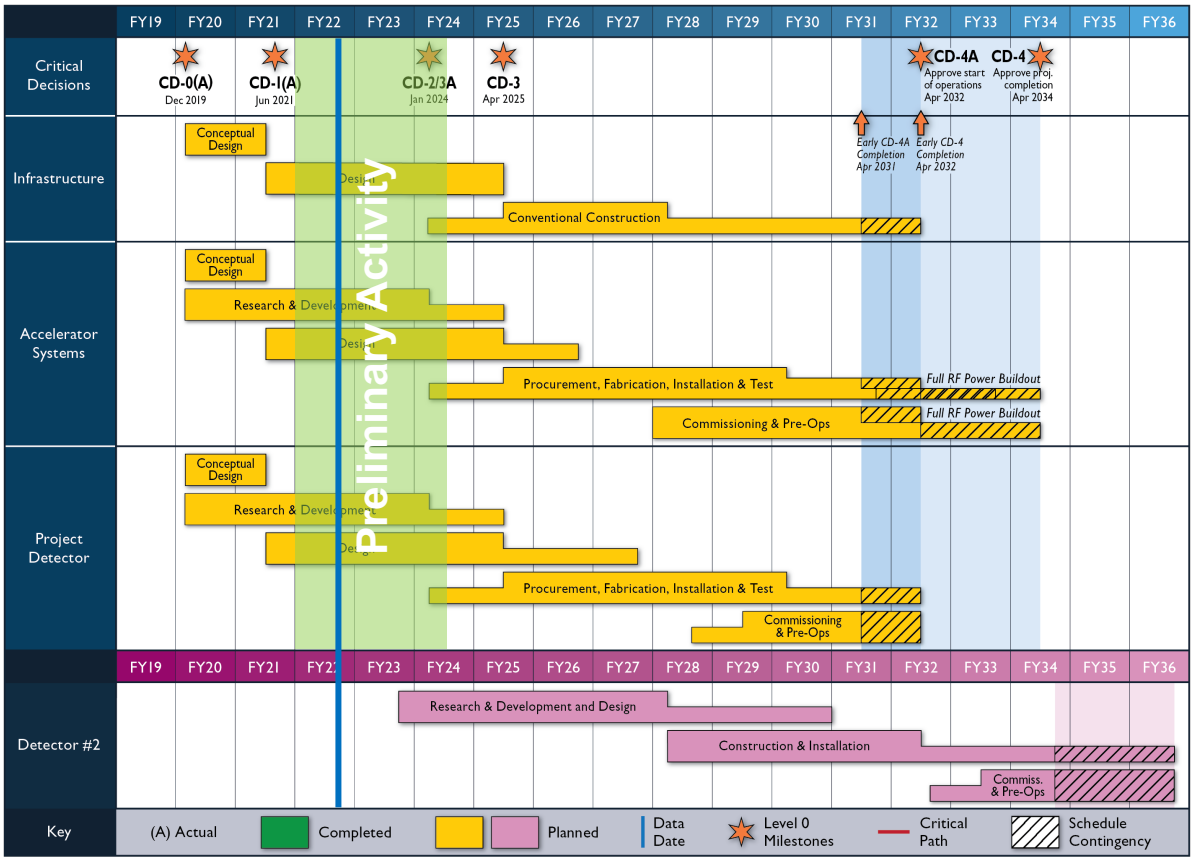


2022: Merging of ECCE and ATHENA proposal strengths forming a new collaboration and a new concept → EPIC experimental collaboration

Starting point: reference detector (i.e. design).

International Project Schedule

NOTE: US Financial Years (FY) = Oct-Sep



UK-EIC Detector R&D Project

UK Track Record

- eRD18/25 – Precision silicon vertexing and tracking for the EIC (2016 – 2021)
  - Laura Gonella, Peter Jones, Paul Newman – Birmingham
  - Iain Sedgwick – RAL TD (Sensor Design Group)
- Yellow Report (Dec 2019 – Mar 2021)
  - Peter Jones – 1 of 4 overall Detector WG Convenors/Editors
  - Daria Sokhan – co-convenor Exclusive Physics subgroup
  - Paul Newman – co-convenor of Detector Complementarity subgroup
- Detector Proposals (Mar 2021 – Dec 2021)
  - Laura Gonella – ATHENA Tracking Detector WG – co-Convenor
  - Paul Newman – ATHENA Inclusive Physics WG – co-Convenor
  - Daria Sokhan – ATHENA Exclusive/tagging Physics WG – co-Convenor
  - Peter Jones – ATHENA Proposal Committee – Editor
  - Nick Zachariou – ECCE Far Backward Detector WG – co-Convenor
  - Claire Gwenlan – ECCE Inclusive Physics WG – co-Convenor
  - Rachel Montgomery – ECCE Exclusive Physics WG – co-Convenor

Current Involvement and Leadership

- EIC Users Group
  - UK has third largest European involvement after Italy and France
  - Currently 35 registered UK users, including 2 accelerator physicists and 1 sensor designer
  - 12 UK institutions: ASTeC/Cockcroft, Birmingham, Brunel, Durham (IPPP), Glasgow, Lancaster, Liverpool, Oxford, STFC RAL (PPD and TD), STFC DL, UCL, York
  - EU Representative on EICUG Steering Committee: Daria Sokhan
- Project Detector Leadership
  - Inclusive Physics WG (Gwenlan, Kutz, Newman, Schmookler)
  - Exclusive, Diffraction & Tagging Physics WG (Klein, Montgomery, Schmidt, Sokhan)
  - Tracking Detector WG (Bossu, Gnanvo, Gonella, Li)
  - Far Backward Detector WG (Jaroslav, Korover, Piotrzkowski, Zachariou)
- EIC Silicon Consortium
  - Leadership team – Laura Gonella (Birmingham), Iain Sedgwick (RAL TD), Ernst Sichtermann (LBNL), Giacomo Contin (INFN Trieste), Domenico Elia (INFN Bari), Grzegorz Deptuch (BNL)

Aspiration for the Construction Phase

- Three detector WPs: MAPS, Timepix and Polarimetry
- MAPS: 65 nm wafer-scale sensors; co-development with ALICE-ITS3. Build 33% of central tracker – vertex and barrel layers, plus possible contribution to forward / backward disks. Technology already adopted in baseline detector.
  - Institutes: Birmingham, Brunel, Lancaster, Liverpool, STFC RAL (PPD and TD), STFC DL
- Timepix: low-Q2 tagger using Timpix4 pixel sensors. Build two tracking stations in far backward region. Detector is baseline. Timepix is a candidate technology.
  - Institutes: Glasgow, STFC DL
- Polarimetry: current activity is exploring use of novel polarised scattering media using chemical hyperpolarization. Nucleon polarimeter is not currently in baseline detector. Also, leading design of electron beam luminosity monitor.
  - Institutes: York