ATLASPix Development for Higgs Factories and Beyond

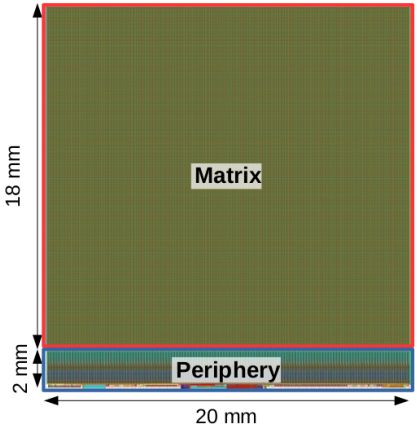
Lingxin Meng, on behalf of many people
from Bristol, Edinburgh, Lancaster, Liverpool, RAL, KIT, Milan, IHEP

Future UK Silicon Vertex & Tracker R&D Workshop
https://indico.stfc.ac.uk/event/592

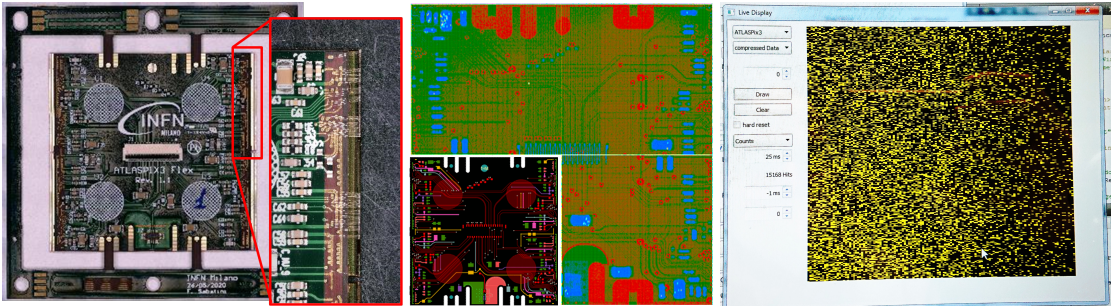
7 September 2022

Introduction

- ATLASPix developed as the HVCMOS pixel sensor candidate for the ATLAS Inner Tracker (ITk) upgrade
- AMS/TSI 180 nm technology on 200 Ωcm wafers with large fill-factor charge collection wells
- Version 3 is the first full reticle-sized sensor for construction of multi-chip modules
- 20.2$\times$21 mm^2 reticle size, 132 columns $\times$ 372 rows, 150$\times$50 μm^2
- RD53 compatible: with command decocer, Aurora protocol, data link up to 1.28 Gbit/s, shunt-LDO regulators for serial powering
- Low power: 160 mW/cm^2 (of which 120 mW/cm^2 is analog) - compared to 500 mW/cm^2 for ITk Pixel
- Low threshold: down to 400 e
- Low material: monolithic, thinned to 150 μm
- Radiation tolerant up to $\sim$1e15–1e16

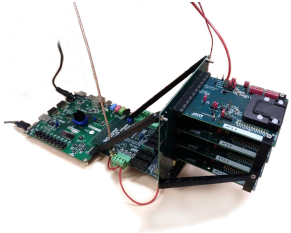


Quad Module

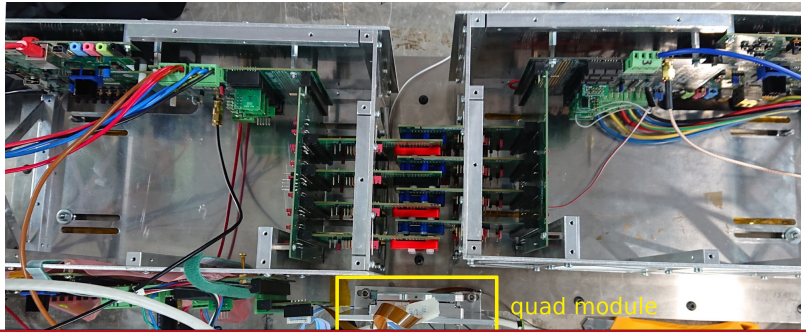


- Quad flex design inspired by ATLAS ITk Pixel
- Quad module assembly by hand and being tested in Milan
- Source measurement with x-ray (5 min with 15k–34k hits/s, untuned threshold)
- First quad in testbeam (display shows one chip in a quad)

ATLASPix3.1 Telescope at Testbeam



- GECCO system with telescope adapter card (4 planes in 2.54 cm pitch)
- All planes share the same HV and LV (voltages can be fine-tuned for each plane if regulators are used)
- 2 arms synchronised, quad module in the beam



Collaboration

- KIT, Germany
  - Chip designer Ivan Peric, over 20 years experience in HVCMOS/MAPS chip design, knows the AMS/TSI process very well, designed many other chips: MuPix, MightyPix...
  - Readout system GECCO: hardware, firmware, software
- INFN Milan
  - Quad flex design, quad assembly and testing
- From the UK (a lot of expertise from different experiments, but very little time)
  - Edinburgh and Bristol: single chip characterisation
  - RAL: software development, testbeam reconstruction
  - Lancaster: single chip/testbeam setup, data reco and analysis
  - Liverpool: wirebonding, stave design, cooling

Status of ATLASPix3(.1)

Lancaster University

- Single chip thoroughly characterised, multi-chip (quad, telescope) shown working
- Chip (and its previous prototypes) proven to be working well, even radiation tolerant, can be taken out of R&D phase and move into production (with a few final iterations)
- Experience and lessons learned from ATLAS ITk Pixel production
- Targeting CEPC silicon tracker, but can also work in any other future tracker
  - e+e-: low material budget, low cooling requirement
  - hh: radiation tolerant
- Production
  - monolithic CMOS allows to produce large areas fast and cheap
  - Established technology in automotive industry $\rightarrow$ optimised process and price, long term availability
  - Quick turn-around time: production capacity of typical CMOS foundries $\sim$10k wafers/month, enough for 100 m^2 with yield and spares
  - Typical price: $\sim$1000 EUR/wafer for large quantities, depending on the process and details

Summary and Outlook

- Matured full reticle-size chip
- Working source and testbeam measurements in single and multi-chip setups
- Lab measurements for more understanding and characterisation of the chip to build more expertise within the UK
- A lot of peripheral development around the chip still needed
  - TB reco and analysis ongoing
  - Improve and automate synchronisation of telesccope arms
  - Development of software frameworks
  - Minor change (wish list) for the next iteration of the chip
  - Integration into faster readout frameworks (e.g. YARR for ATLAS ITk Pixel)
  - ...
- Need a lot more effort (experts) to carry it forward
  - Open to new collaborators
- All in all good large area tracker candidate for Higgs factories and general future experiments

References

- ATLASPix3 Manual
- R. Schimassek, Test results of ATLASPIX3 A reticle size HVCMOS pixel sensor designed for construction of multi chip modules
- Telescope public wiki: https://git.scc.kit.edu/adl_publicsoftware/atlaspix3_public/-/wikis/Telescope-Revision-2-Wiki-Main-Page

backup

ATLASPix3(.1)

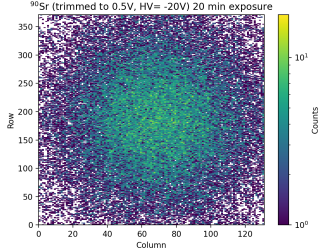
Lancaster University

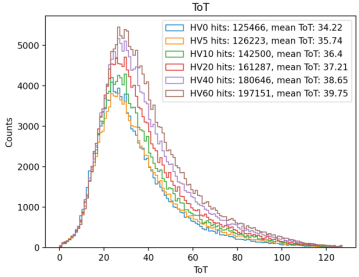
- 3-bit threshold TDAC, 8-bit ToT, 10-bit time stamp (extended by 30 more bits from the FPGA)
- Voltage regulators for shunt-LDO operation in serial power chains
- Column-drain readout with and without trigger (triggered and hit-driven)
- Configurable through serial, SPI bus or command line
- RD53 compatibility
  - Data encoding w Aurora protocol (triggerless: 8/10b, triggered: 64/66b)
  - Data link up to 1.28 Gbit/s
  - Command decoder
- Low power $\rightarrow$ less requirement on cooling: 160 mW/cm^2 (of which 120 mW/cm^2 is analog) - compared to 500 mW/cm^2 for ITk Pixel
- Low threshold: down to 400 e
- Low material budget apart from being monolithic: thinned to 150 μm
- Version 3.1 currently with changes on the metal layers
  - \+ Biasing structure of the pixels: to remove a potential cause of early breakdown
  - \+ Time-walk by reducing ($\sim$halving) the input capacitance of the amplifier
  - \+ Voltage regulators (VDD) to avoid oscillations by adding capacities
  - \- Shielding of the test signal injection due to restructured metal layers resulting in crosstalk

Single Chip Measurements

- Readout using GECCO (GEneric Configuration and COntrol) system for single chip, quad and telescope
  - Diligent Nexys Video FPGA board + firmware
  - GECCO board (middle) with function card slots
  - Single chip card (can be swapped out)
  - Qt-based software GUI
- Source (Sr90) measurements at different bias voltages

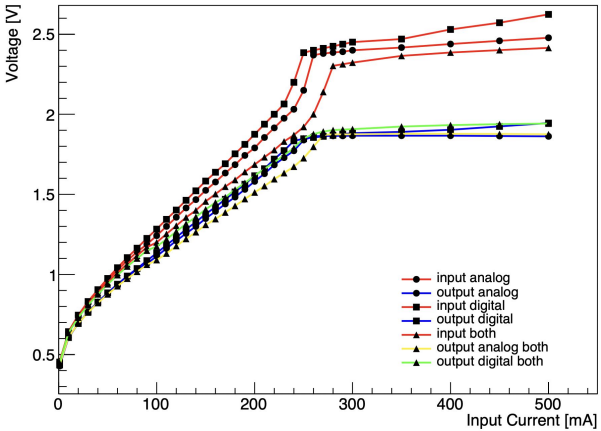
Single chip setup in Edinburgh





Regulator Characterisation

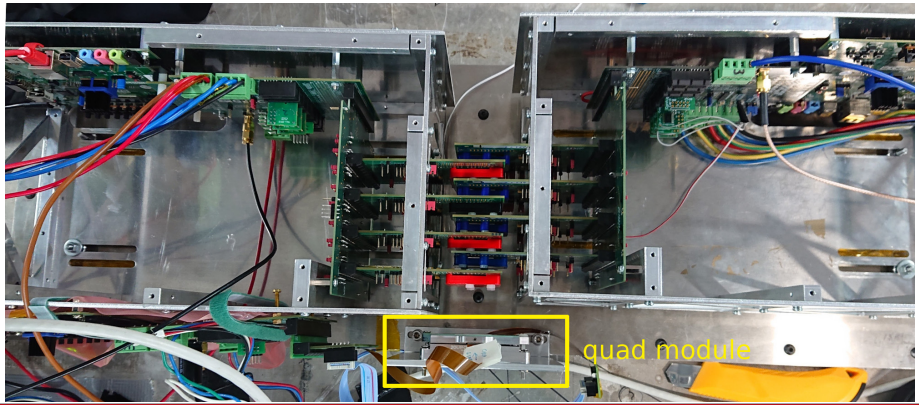
- 6 low voltages needed for readout, 1 high voltage for bias
- All LV can be generated on-chip
- Main VDDA/VDDD for shunt-LDO operation
- Test done on a single chip card
- Output values matching 90 mA analog current and 223 mA digital current



(Milan)

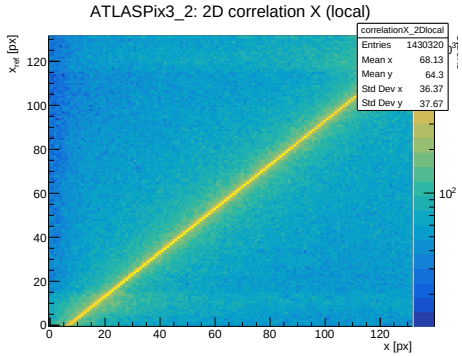
Testbeam at DESY

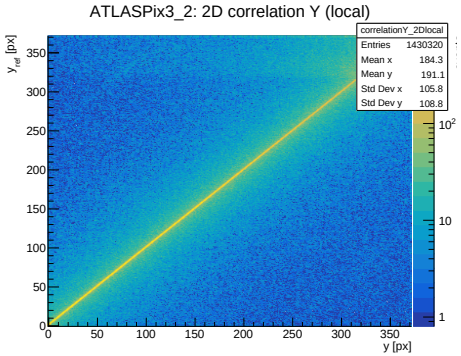
- Testbeam at DESY in April using 6 GeV electron beam
- 2 arms in 2 standalone systems, biased at $\sim$ 50 V
- Synchronisation provided by the primary system sending sync signal to the secondary
- Using hit-driven readout
- Interleaved arms with 1.27 cm distance between planes
- Quad module in the beam (bottom, in the pixel module carrier)



Testbeam Reconstruction

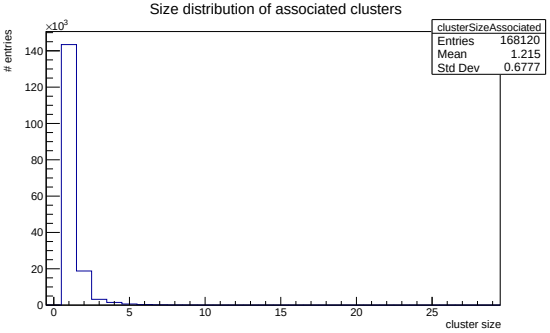
- Ongoing progress to understand the data and develop software frameworks
- Improved decoder to convert from binary to human-readable data, compatible with Corryvreckan input format
- Improved ATLASPix3 eventloader in Corryvreckan
- Developed automated reco scripts, fine-tuning the parameters

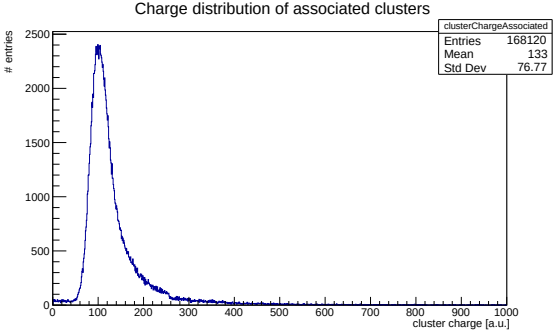




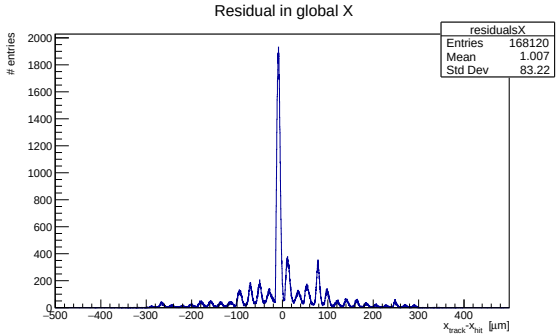
Reconstruction of a Long Run at 6 GeV

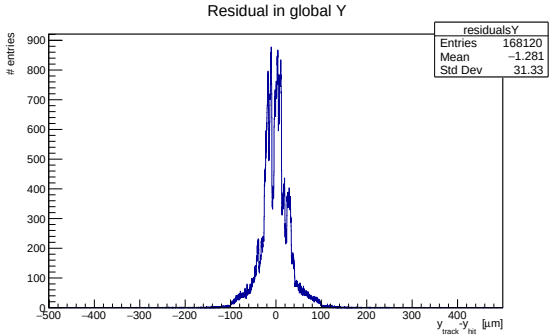
- Use L1,2,4 as telescope planes and run telescope alighment with increasing number of tracks and decreasing spatial cuts
- Use L3 as DUT and run DUT alignment with increasing number of tracks and decreasing spatial cuts
- DUT and efficiency analyses (ongoing)





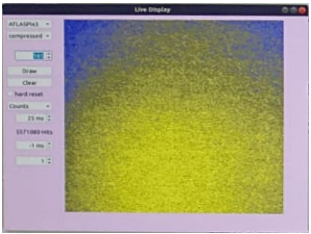
DUT Global Residuals



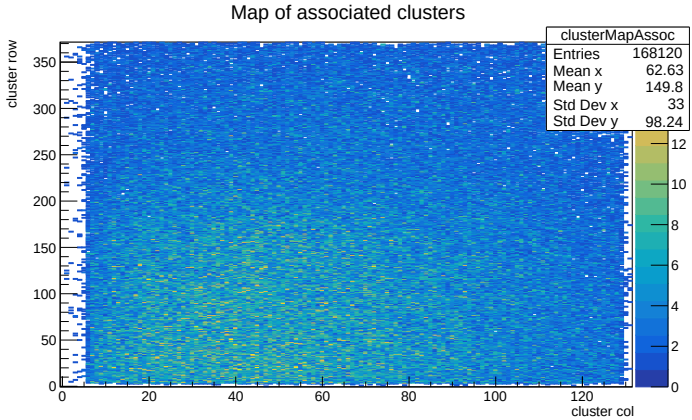


Peak structure from large pixel width and mostly single-pixel clusters

DUT Cluster Map



Live event display at TB
(all layers accumulated,
different run/geometry)



Beamspot seen on DUT