CMOS sensor for the LHCb Mighty Tracker and RD50

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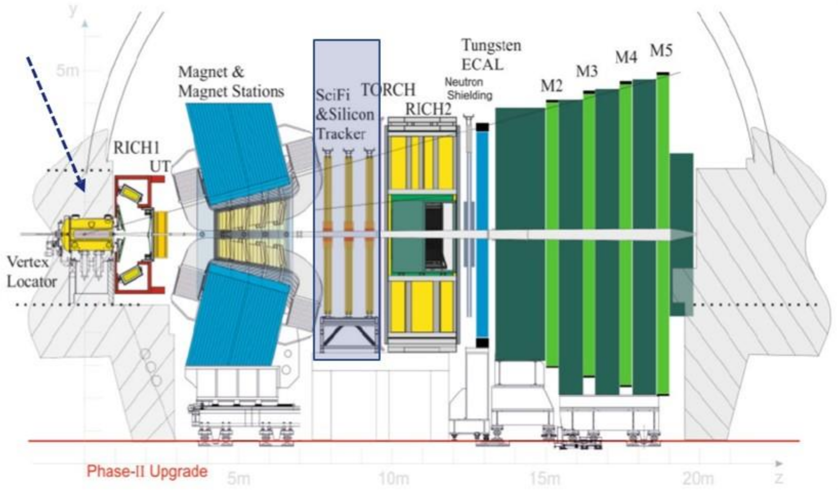
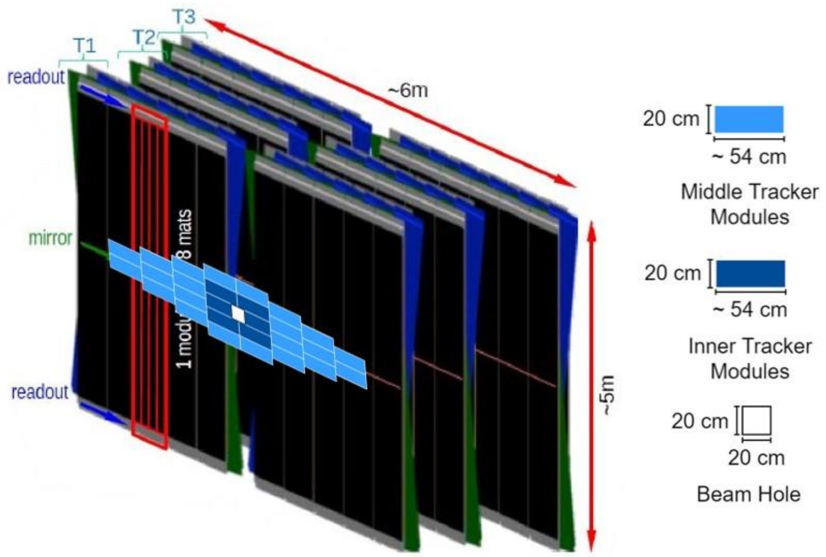
The Mighty Tracker at LHCb

- Upgrades of the detector systems are required to cope with the increased luminosity anticipated in the coming runs

- Proposed hybrid tracker composed of
  - **Scintillating Fibre Tracker (SciFi)**
    - Scintillating fibres with SiPM readout
    - Installed in LS2, replacements in LS3
  - **Inner Tracker (IT) and Middle Tracker (MT)**
    - **Monolithic High Voltage-CMOS sensors**
    - To meet the anticipated requirements on granularity, radiation tolerance and cost
    - Installation planned for LS3 and LS4





MightyPix R&D programme

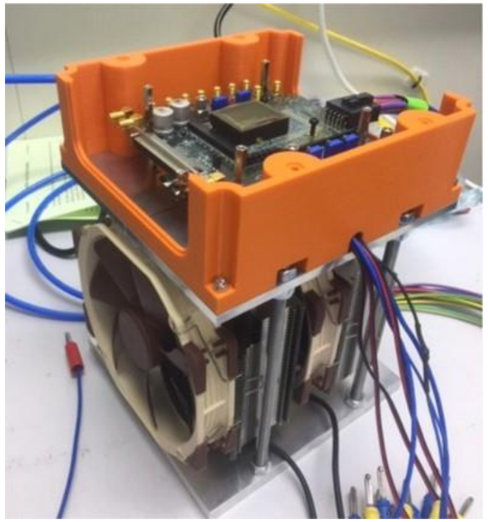
- Dedicated R&D programme to develop a High Voltage-CMOS sensor chip that meets the Mighty Tracker requirements
  - **Pixel size** → < 100 µm x 300 µm
  - **Timing resolution** → ~3ns
  - **In-time efficiency** → > 99%
  - **Radiation tolerance** → 6E14 n_{eq}/cm^2
  - **Power consumption** → < 150 mW/cm^2
  - **Compatibility with the LHCb readout system**
- The programme foresees several High Voltage-CMOS sensor chip submissions
  - **MightyPix1 (2022)** → first prototype dedicated to the Mighty Tracker
  - **MightyPix2 (2023)** → full LHCb engineering run submission (2 cm x 2 cm) & 100% compatibility with LHCb readout system
  - **MightyPix3 (2024)** → production sensor chip for LS3
  - **MightyPix4 (2027-28)** → improved sensor chip for LS4

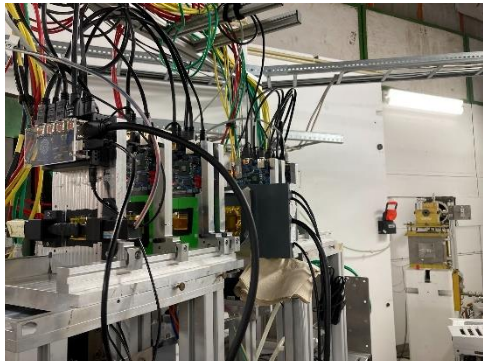
MightyPix1

- **First High Voltage-CMOS sensor dedicated to the Mighty Tracker**
  - Pixel size: 55 µm x 165 µm
  - 320 rows, 29 columns
  - Chip size: 0.5 x ~2 cm
  - ¼ of final MightyPix size → ¼ width, full column length
  - First prototype compatible with LHCb readout system
    - Runs with LHC clock at 40 MHz
    - Uses lpGBT protocol
    - Meets TFC and ECS requirements
  - Designed by KIT with some inputs from Uni. Liverpool
  - Submitted in May 2022 for fabrication with TSI (180 nm node)
  - Delivery expected in December 2022

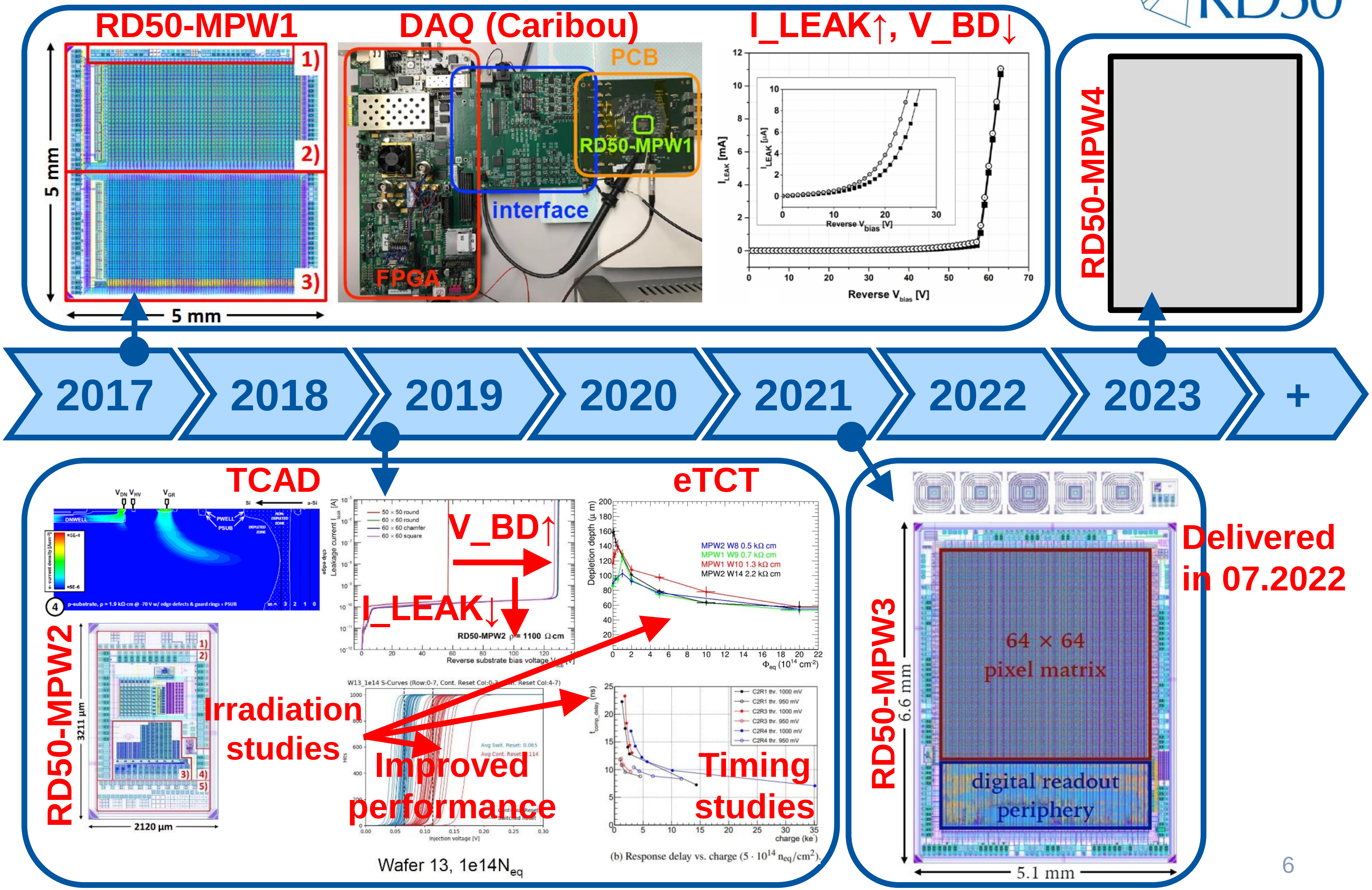
Ongoing evaluation programme

- **Use existing, similar prototypes to evaluate key parameters such as timing performance after irradiation to relevant fluence in both the lab and test beams**
  - Chip used: ATLASPix3.1
  - Full size High Voltage CMOS demonstrator for ATLAS ITk in TSI 180 nm
  - Pixel size: 50 µm x 150 µm
  - Similar analogue front-end architecture as MightyPix
  - Irradiated up to 3E15 n_{eq}/cm^2
  - Evaluated at DESY test beam at three operating temperatures: -10, 0 and +5 °C
  - Analysis ongoing, but results are promising (LHCb note to be published soon)
- **Motivation is to inform the MightyPix mechanics design effort of the best operating temperature to develop a cooling strategy**





CMOS and monolithic devices

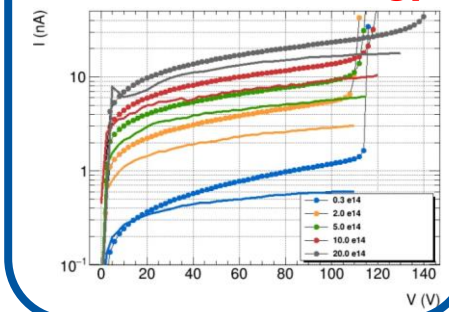


CMOS and monolithic devices

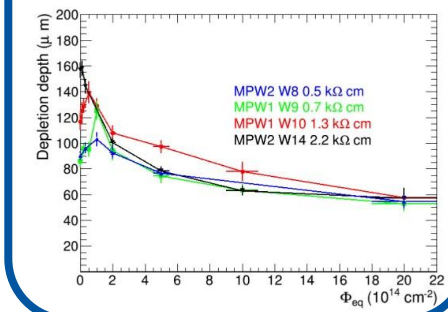
RD50-MPW2: Prototype HV-CMOS sensor with test structures and a small active pixel matrix, fabricated in high resistivity substrates in a Multi-Project Wafer submission with LFoundry.

- Aim to study and improve time resolution and radiation tolerance with high granularity pixels (60 µm x 60 µm)
- Evaluated in the lab before and after neutron irradiation up to 2E15 n_{eq}/cm^2

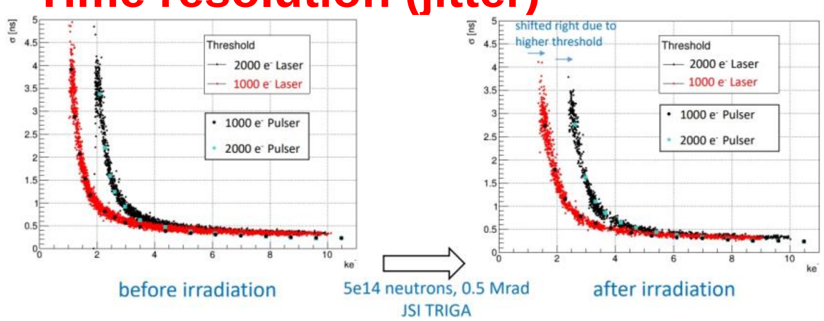
I-V (after 80 mins annealing)



eTCT @ V_HV = 100 V, 2 kΩcm

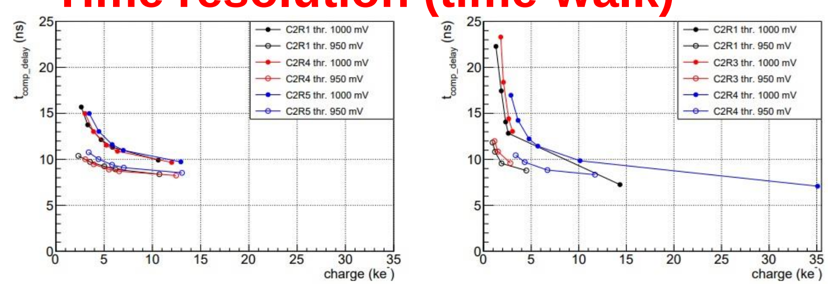


Time resolution (jitter)



Jitter < 160 ps before and after irradiation to 5E14

Time resolution (time-walk)



(a) Response delay vs. charge (unirr.).

(b) Response delay vs. charge ($5 \cdot 10^{14}$ n_{eq}/cm^2).

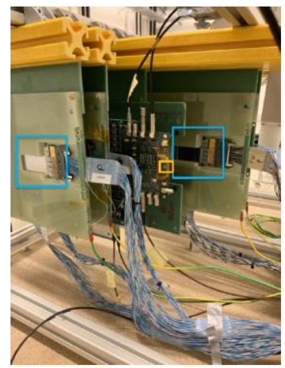
Time-walk < 10 ns before and after irradiation to 5E14 @ > 2ke⁻ collected

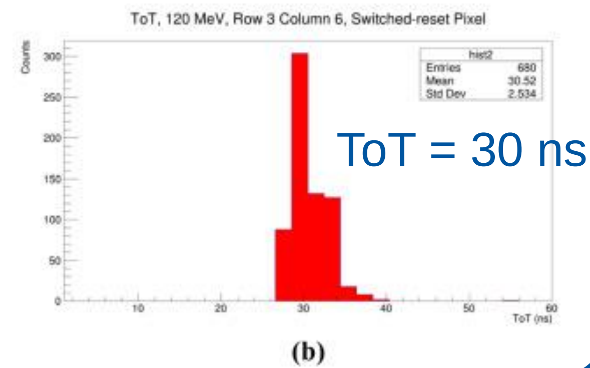
CMOS and monolithic devices

<u>RD50-MPW2</u>: Prototype HV-CMOS sensor with <u>test structures and a small active pixel matrix</u>, fabricated in high resistivity substrates in a Multi-Project Wafer submission with LFoundry.

- Evaluated at proton (medical) and ion beam facilities
- To validate the DAQ and obtain first results

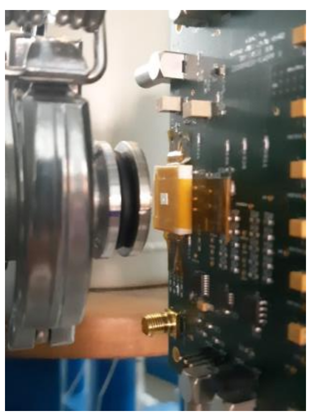
Proton test beam

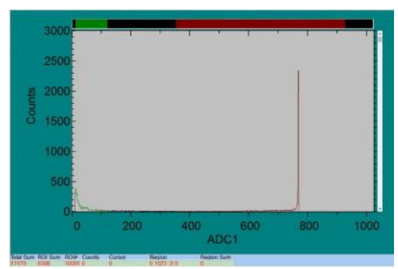


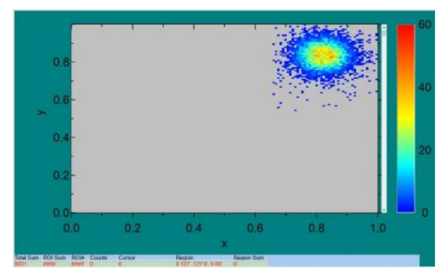


ToT = 30 ns

Ion test beam







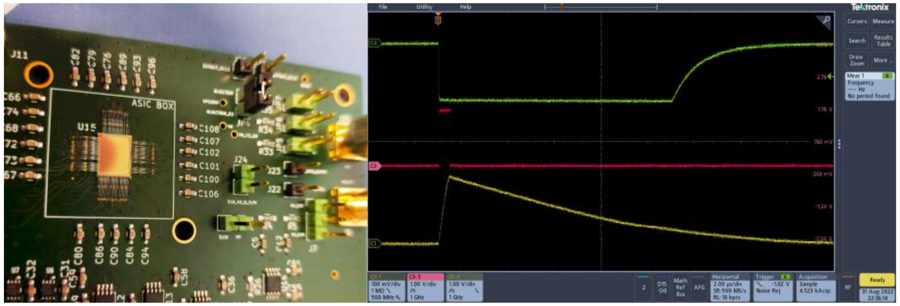
2 MeV proton microbeam
Results suggest the presence of SETs, further studying with simulation tools

CMOS and monolithic devices

RD50-MPW3: Prototype HV-CMOS sensor with advanced test structures and a 64 x 64 active pixel matrix, fabricated in high resistivity substrates in a Multi-Project Wafer submission with LFoundry.

- Improved design to enable a wider range of measurements
- Beam time booked at SPS (10.2022, non-irradiated samples); test beam with irradiated samples planned
- Neutron and proton irradiation campaigns ongoing

Initial lab evaluation is satisfactory (samples delivered in 07.2022)



Improvements include:

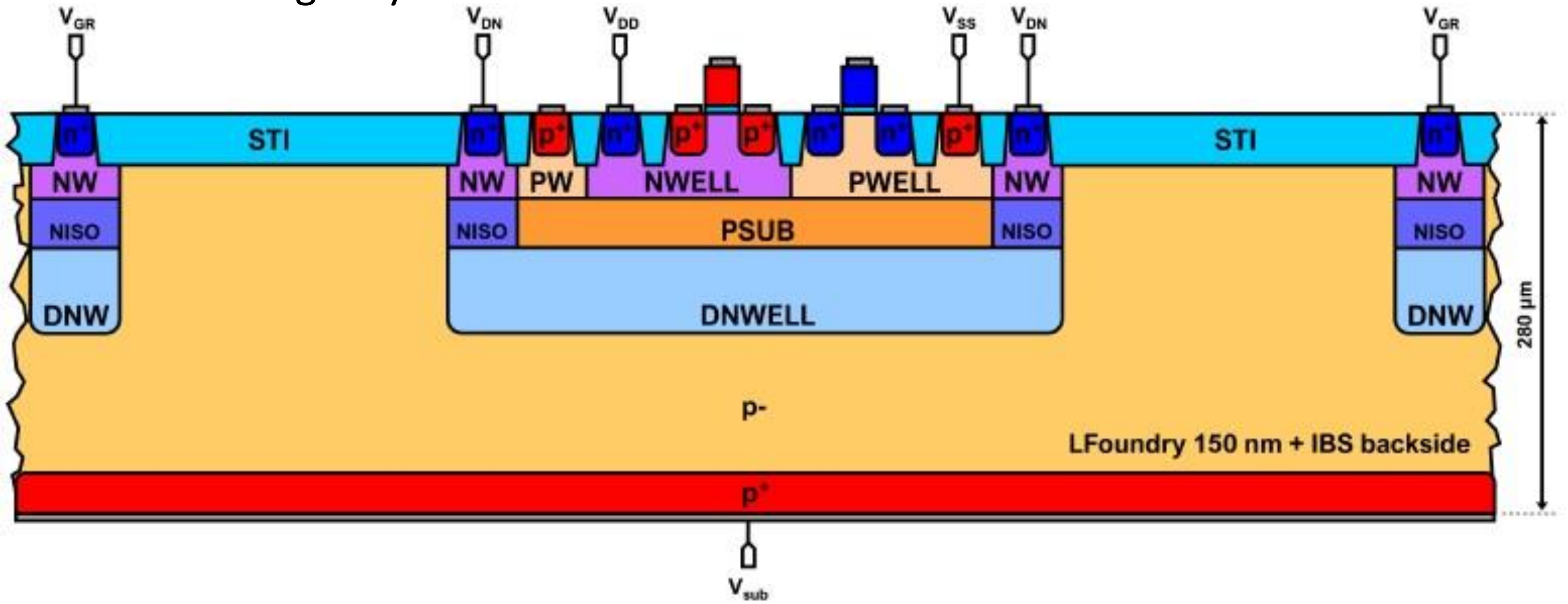
- Larger number of active pixels in matrix (64 x 64 pixels)
- Analogue and digital readout embedded in small pixel area (62 µm x 62 µm)
- Optimised design to minimise crosstalk noise, to speed sensor configuration and to speed data readout
- Advanced test structures with guard rings to further improve I-V and also to evaluate defect concentration before and after irradiation

Future work

- Continue activities to further study and develop the sensor with low-cost submissions
- Evaluate RD50-MPW3 in the lab and in test beams before and after proton and neutron irradiation to high fluence
- Design and submit a new and larger prototype (RD50-MPW4) with all the lessons learned so far
- Optimise the design with backside biasing for operation beyond E16 n_{eq}/cm^2
- Evaluate RD50-MPW4

Generic R&D at Uni. Liverpool

- UKRI-MPW0 → LF15A MPW chip submission with High Voltage-CMOS pixels
- Main motivation
  - Particle physics experiments where high radiation tolerance is required
  - Achieve a very high V_BD to improve radiation tolerance
- UKRI-MPW0 has new cross-section that uses backside biasing only
  - No shallow p-type layers in direct contact with the substrate
  - Substrate backside biasing only



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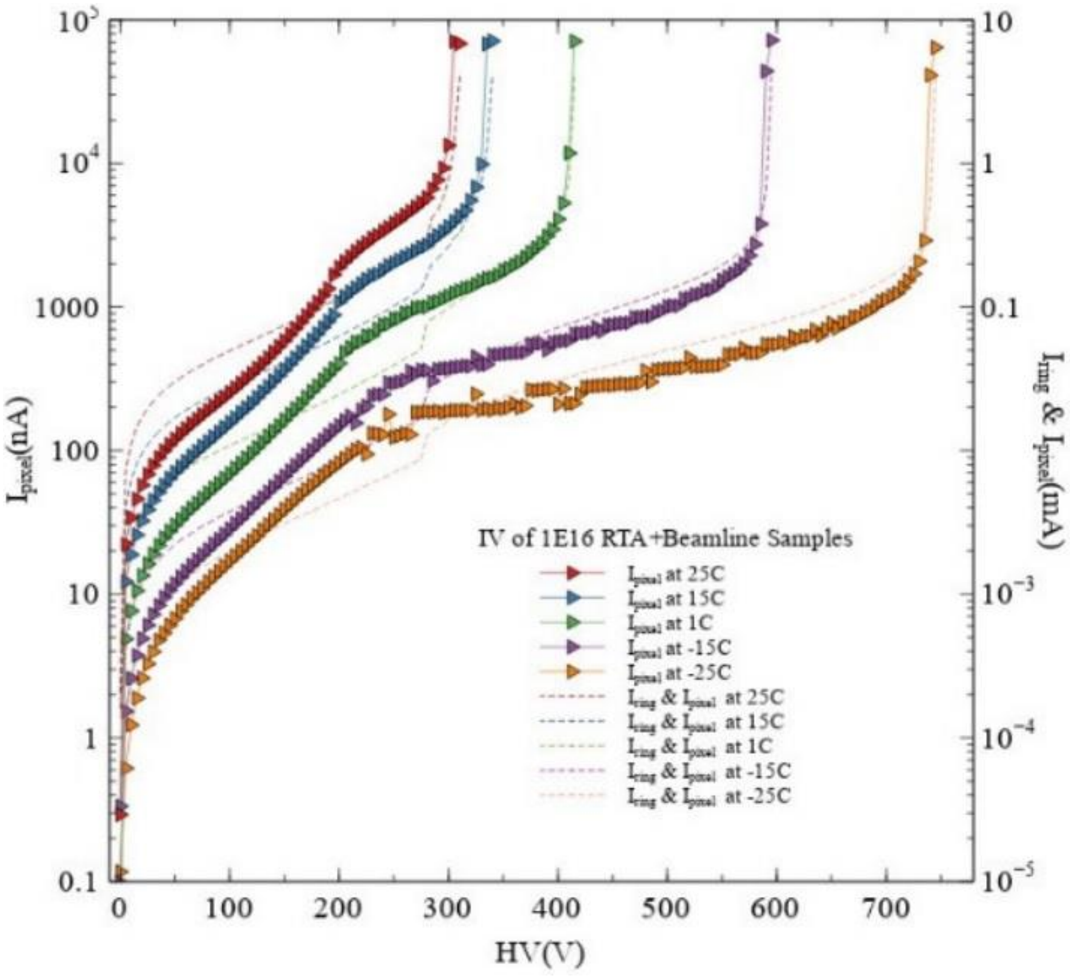
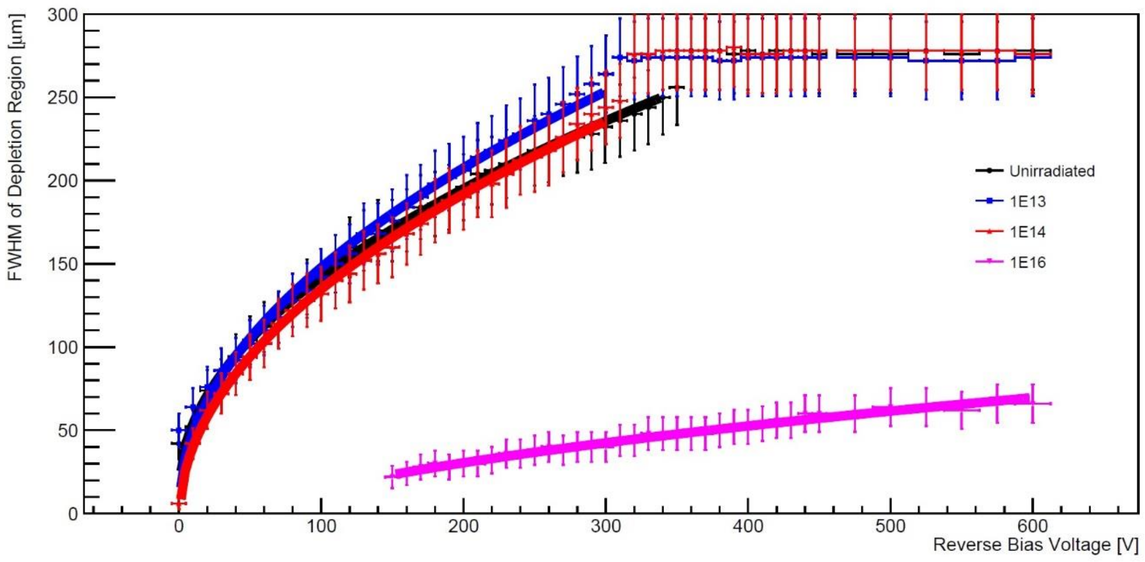
Generic R&D at Uni. Liverpool





Preliminary