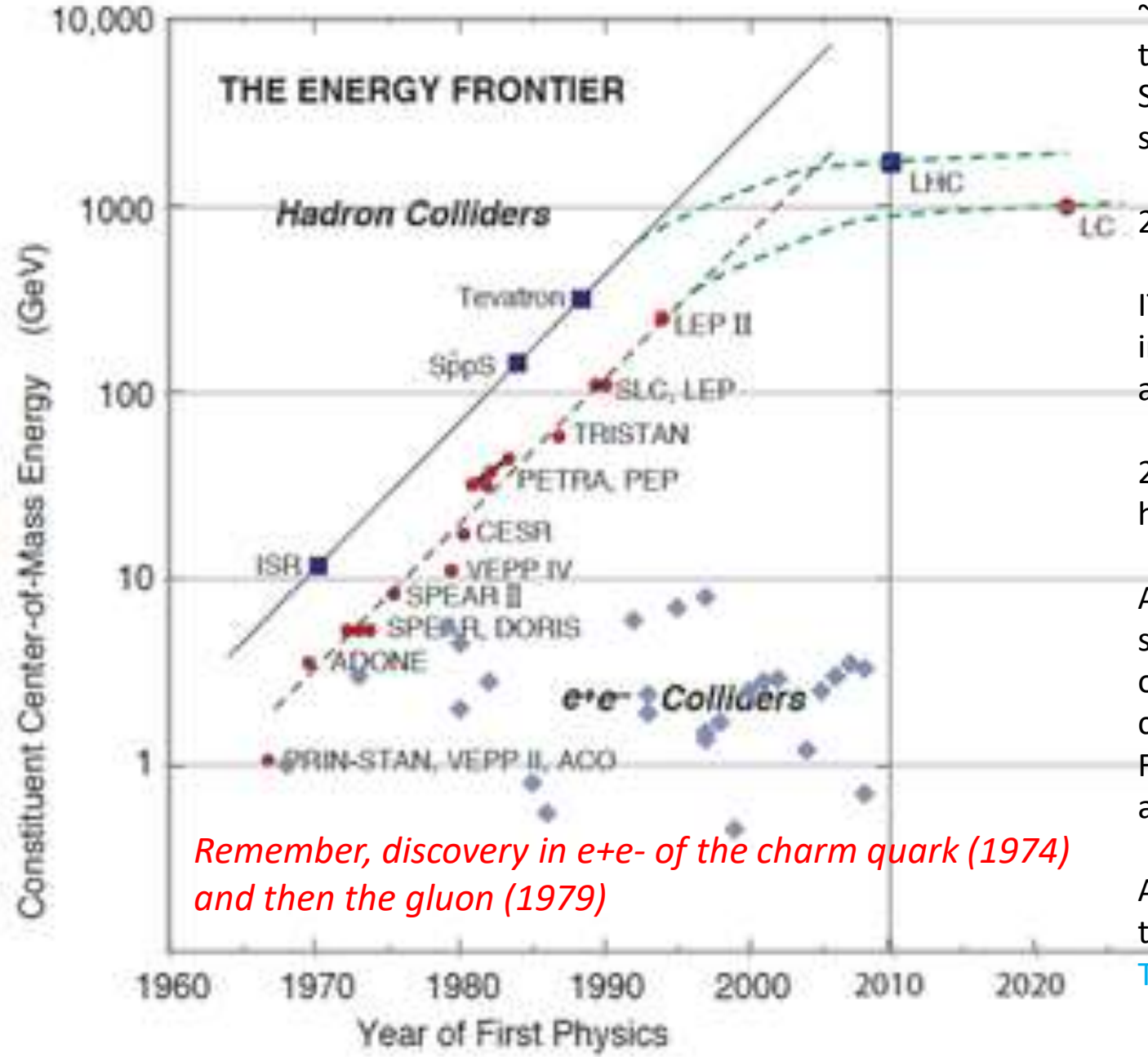
An ultra-low-mass silicon pixel tracker for ILC or C^3

[C-cubed, a 'Cool Copper Collider' – SLAC, LANL, UCLA, INFN-Frascati, FNAL]

Chris Damerell
RAL
16 Feb 2022

- ILC and C^3 status, two options for a TeV-scale e+e- linear collider now under discussion at Snowmass
- SPT: A Silicon Pixel Tracker of minimal material, matched to both these accelerator concepts



Remember, discovery in e+e- of the charm quark (1974) and then the gluon (1979)

Synopsis of the mammoth ILC saga:

~1990, SLC/SLD working at last. Stimulus for the next step to become real, in form of NLC, TESLA, JLC and CLIC. At Saariselka, the first international workshop, Bjorn Wiik suggested first physics ~2000, hosted by DESY

2003, TESLA was dropped; DESY to focus on EUXFEL

ITRP formed (Barry Barish) and recommended SCRF option in 2004. Most labs cooperated to make it work, with FNAL as the natural host.

2008 DOE/FNAL dropped it; Japan provisionally offered to host, and most labs cooperated on this.

After 14 long years, there's opposition from KEK, and scepticism from MEXT, who see ILC as a 3-legged stool with one weak one. 'Europe seems not to be interested'. They could be right - many in Europe are happy to focus on FCC-ee, a wonderful Higgs Factory, but which risks creating a cul de sac in terms of the energy frontier.

A recent twist: is SCRF still the preferred technology, given the exciting developments in 'cool copper': C-cubed? There's always room for a good idea.

High energy lepton collider concepts(9)

Footprint 31 km for 500 GeV

Name	Nominal COM energy and peak luminosity per IP at nominal energy
High Energy ILC	e+e-, $\sqrt{s}$ = 3 TeV, L= 6.1 ×10^{34}
High Energy CCC	e+e-, $\sqrt{s}$ = 3 TeV, L= 6.0 ×10^{34}
High Energy CLIC	e+e-, $\sqrt{s}$ = 3 TeV, L= 5.9 ×10^{34}
High Energy ReLiC	e+e-, $\sqrt{s}$ = 3 TeV, L= 33 ×10^{34}
MC – Proton Driver	$\mu\mu$, $\sqrt{s}$ = 3 TeV, L= 2.25 ×10^{34} *
MC – Fermi site filler	$\mu\mu$, $\sqrt{s}$ = 6 – 10 TeV, L= 20 ×10^{34} *
LWFA-LC (e+e- and $\gamma\gamma$)	Laser driven plasmas; e+e-, $\sqrt{s}$ = 1 – 30 TeV
PWFA-LC (e+e- and $\gamma\gamma$)	Beam driven plasmas; e+e-, $\sqrt{s}$ = 1 – 30 TeV
SWFA-LC	Structure wake fields; e+e-, $\sqrt{s}$ = 1 – 30 TeV

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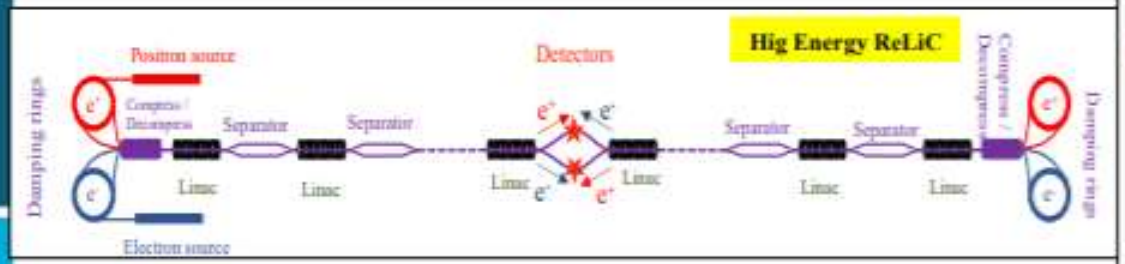
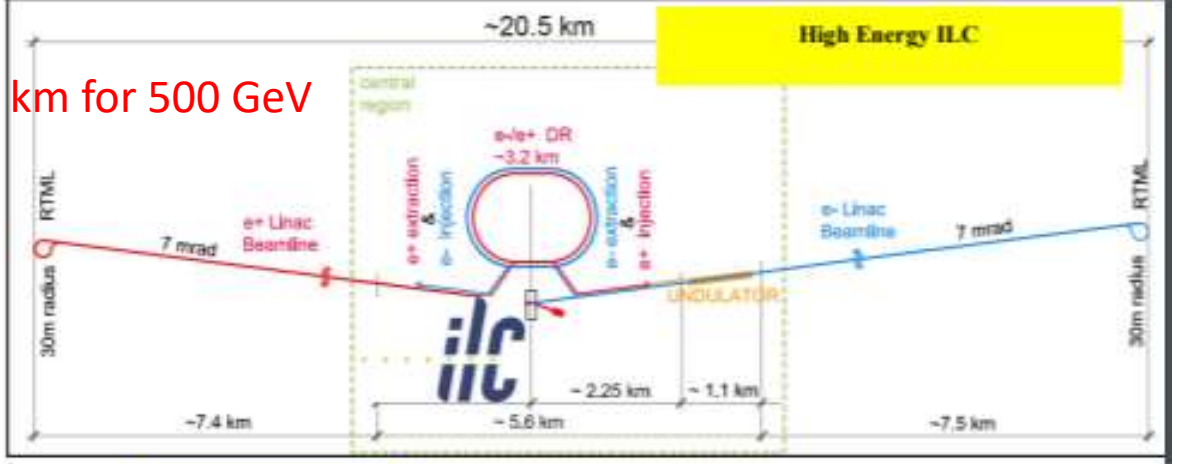
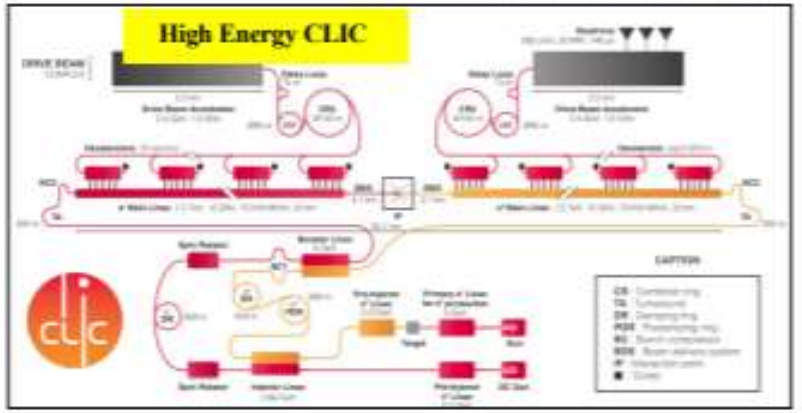
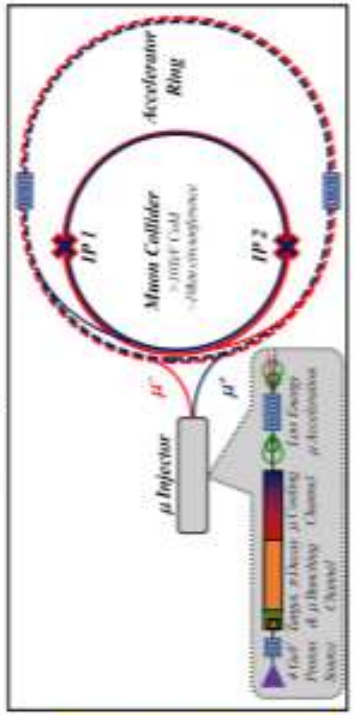
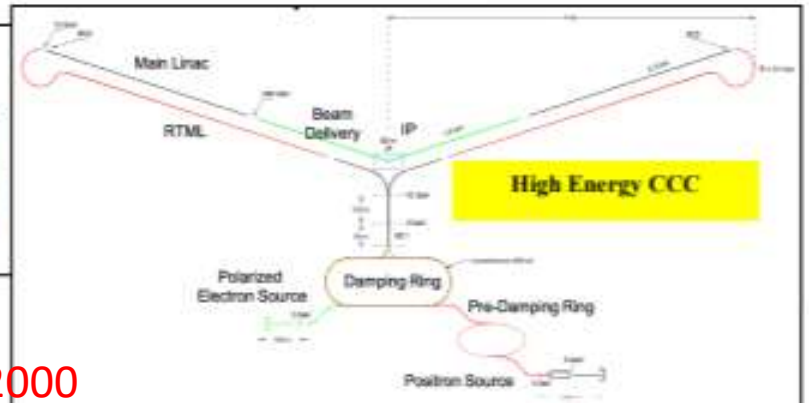








μ+μ- 10-14 TeV cme
10-14 km, 16 T magnets



Brookhaven National Laboratory

* Detector 'an aspiration' KL
No change since Bob Palmer ~2000

Footprint 8 km for 550 GeV

Thomas Roser, 18 Jan 2022
Snowmass

- In 2004, NLCTA was ‘melting a lot of copper’. ITRP decision in favour of SCRF was reasonable at the time

- Ongoing progress with room-temperature high-gradient accelerators has been driven by many commercial applications, including need for compact X-ray sources for baggage checking.

- Emilio Nanni and colleagues at SLAC devised a new approach for the e+e- energy frontier – the Cool Copper Collider

- The key features are:

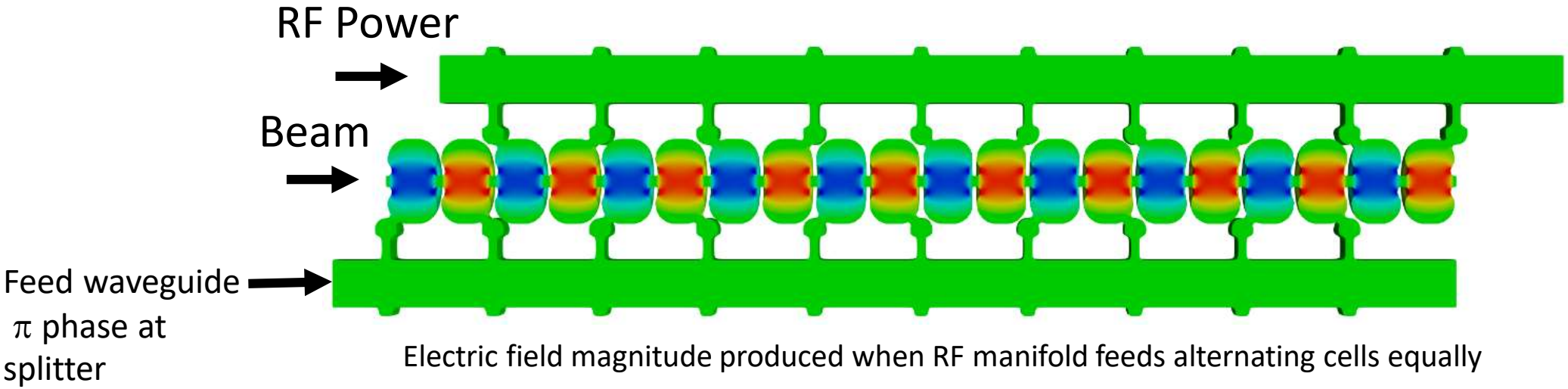
    - Modified accelerating structures – ‘separated function’ *for every cell*: large aperture for power delivery, plus small beam apertures, leading to reduced peak fields

    - Operation at low temperature (liquid nitrogen, which is cheaper than milk) for greatly reduced surface resistance

- Can then raise the accelerating gradient to ~150 MV/m, compared with 31.5 MV/m for ILC (superconducting niobium)

Breakthrough of Distributed RF Coupling Changes the Paradigm for RF Accelerator Performance

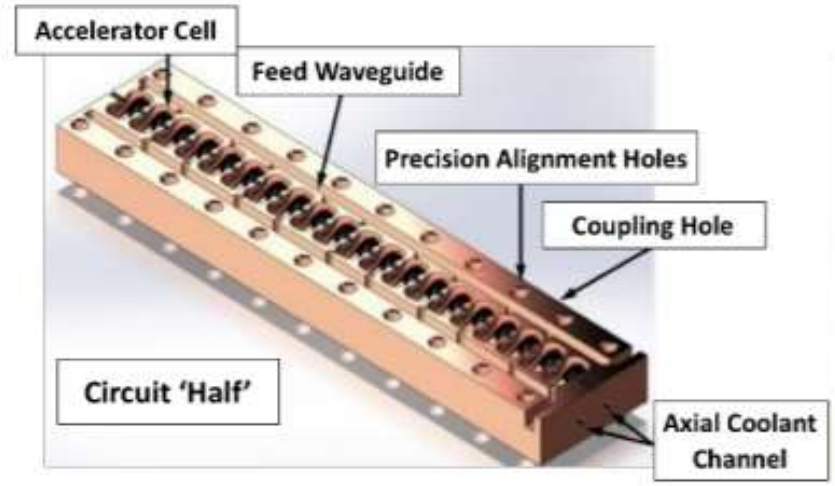
- RF power coupled to each cell – no on-axis coupling
- Full system design requires modern virtual prototyping

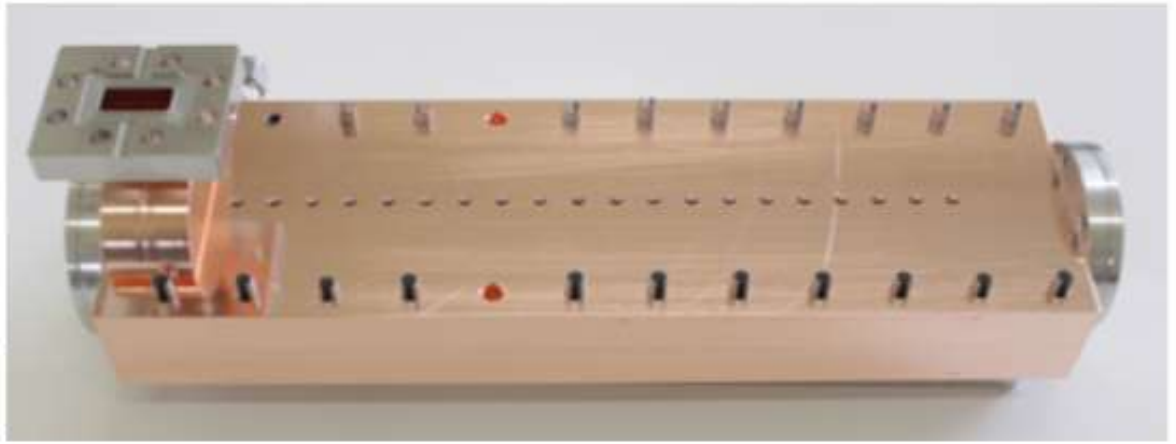


Electric field magnitude produced when RF manifold feeds alternating cells equally

- Beam aperture only 2.62 mm radius
- Control peak surface electric and magnetic fields by optimal cell design
- Key to high accelerating gradient

Emilio Nanni, SLAC. ArXiv 2110.15800 (2021)



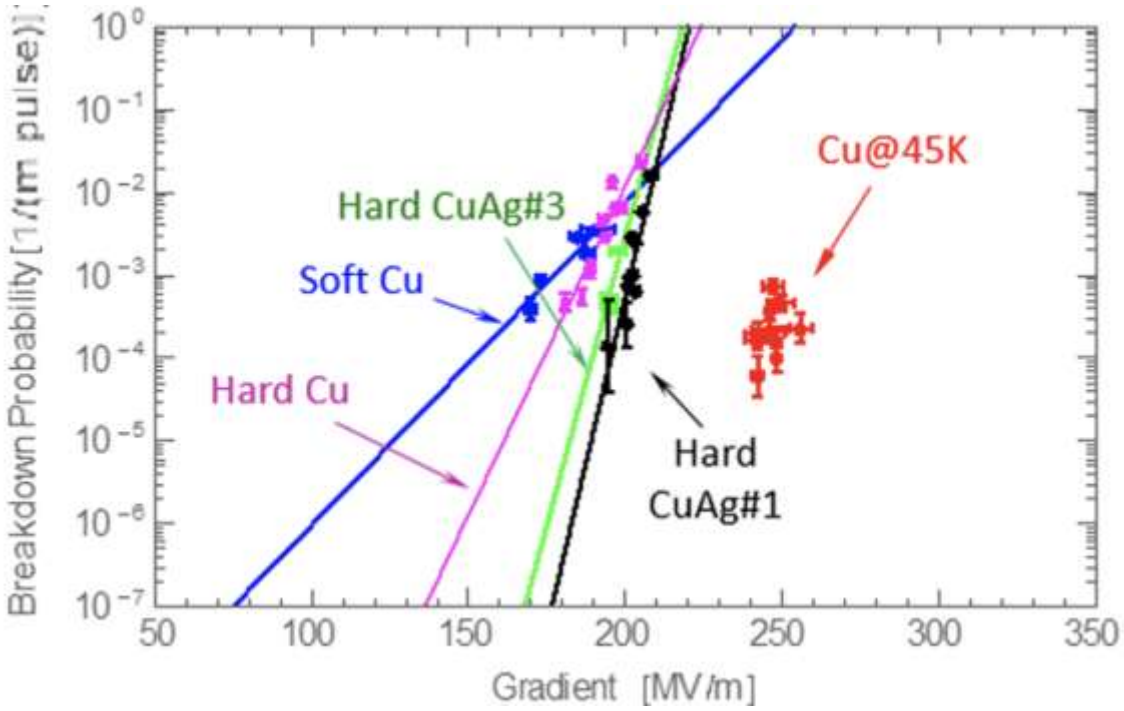


Prototype accelerating structure (half-length - 50 cm long, 20 cells):

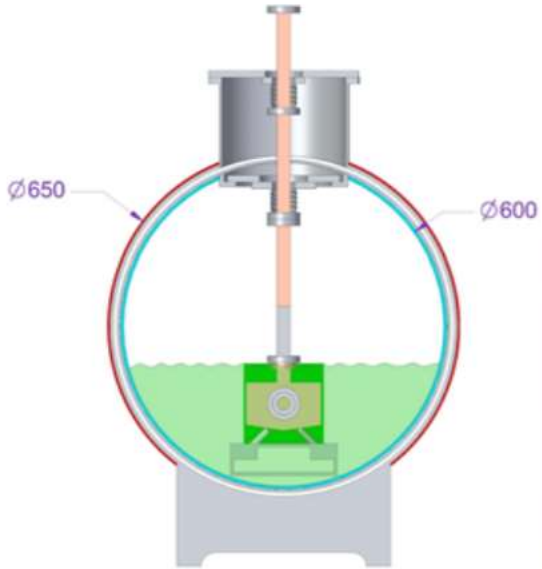
- Split-block fabrication: 2 copper slabs (no current crosses the mid-plane)
- State-of-art CNC machining – inexpensive mass production, no post-CNC finishing required
- Tested up to 160 MV/m, including with beam
- Robust compared with SC cavities, where the risk of operational accidents (such as the fire in SLC DR and the splice joint failure at LHC), plus earthquake damage, are ongoing concerns. [Even if exposed to smoke, copper cavities can be cleaned by 'beam scrubbing'. Not so for superconducting cavities.]

Transformative Impact for Efficient High-Gradient Operation with Cryo-Copper Accelerators

- Surface resistance of copper at 5.71 GHz is reduced by factor 2.55 when cooling from 300 K to 77 K
- Operation with liquid nitrogen is simple and practical



Cahill, A. D., et al. *PRAB* 21.10 (2018): 102002.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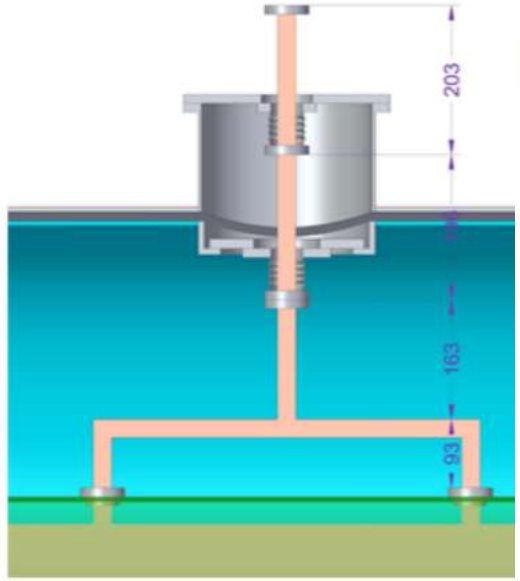
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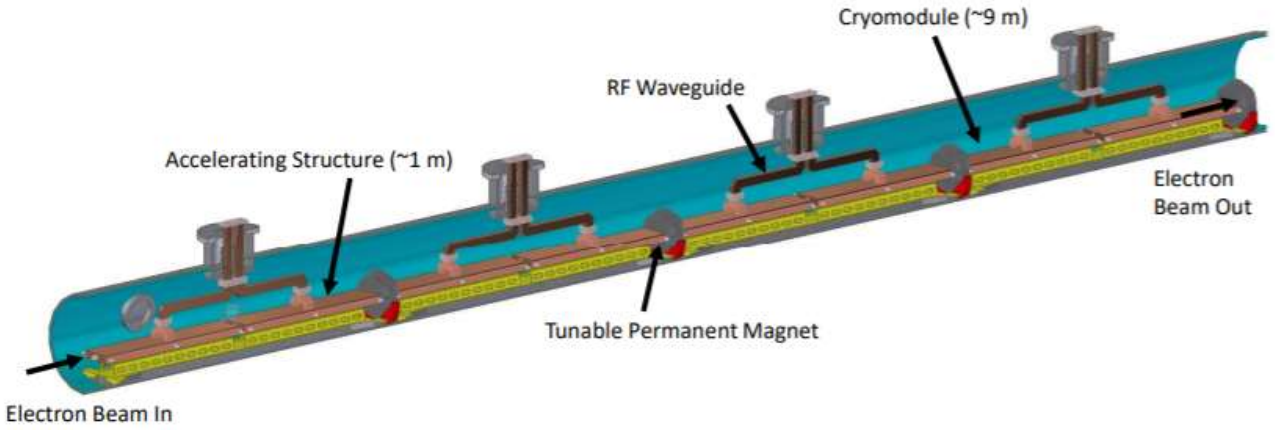
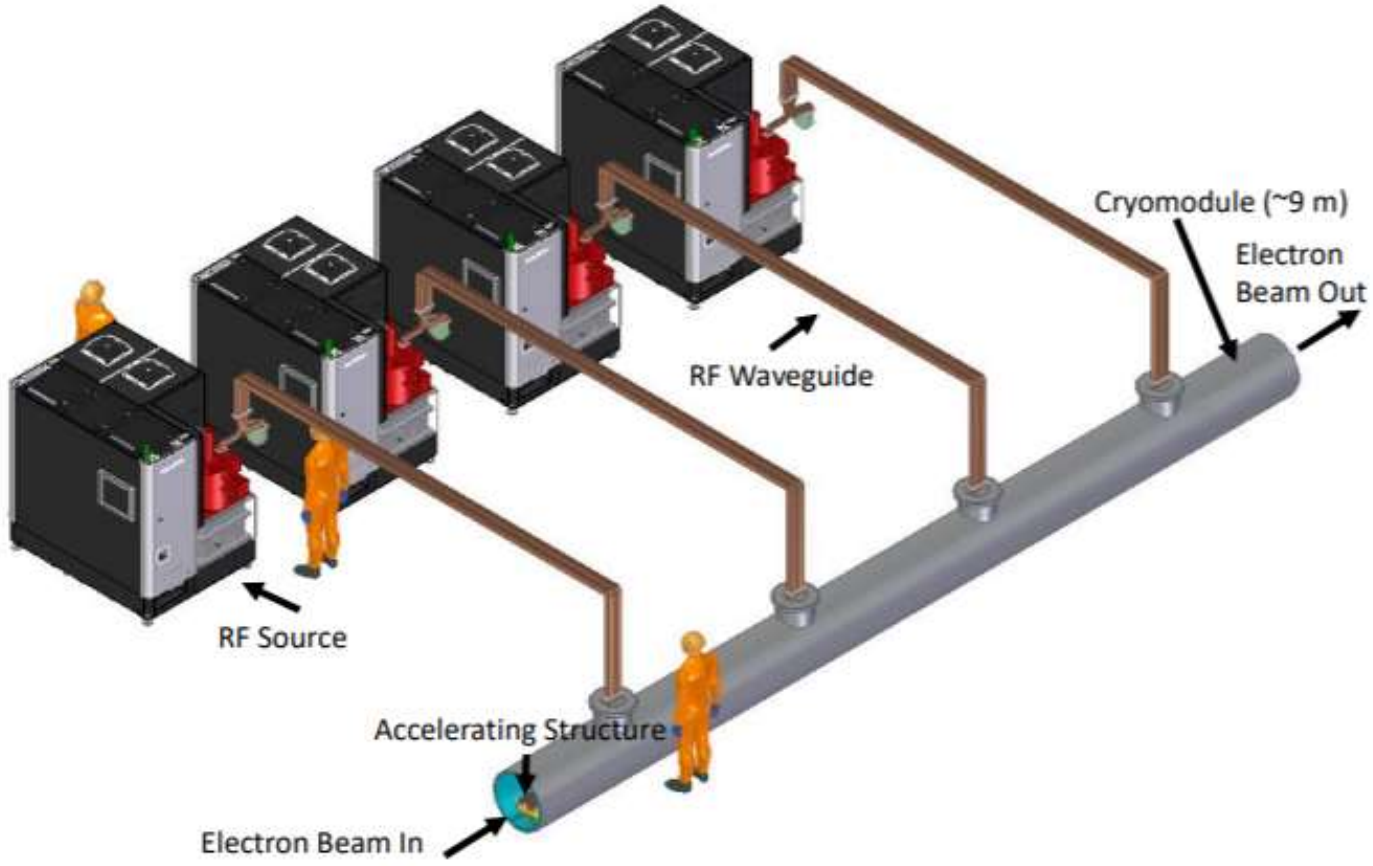


Next step (when funded) will be a complete cryo-module (8 of 1 m accelerating structures)

Fed by 4 commercial RF sources, C-band klystrons, which are steadily becoming more efficient and less expensive (Powerful world-wide collaboration between CERN, KEK, PSI, INFN, SLAC, Fermilab, IHEP, … and industry)



Next steps for C^3

- Would be helped by an authoritative comparison with ILC (hopefully without convening another ITRP). We hope to get an impartial expert (someone of the stature of Reinhard Brinkman) during the 'Collider discussions' sessions at Snowmass, 28-31 March, to provide a technical comparison between ILC and C^3

- Needs ~$100 M to produce a full cryo module (meanwhile, costs continue to fall, with ongoing klystron development)

- Will need strong backing from DOE and the next Fermilab Director, in contrast to the 'hadron alliance' in 2008, which convinced the authorities to kill off the previous US-based proposal. Hoping to avoid further 'scientific vandalism'. The Fermilab Site Filler Collider working group has given encouragement

- Provisional schedule has 250 GeV machine operating from 2040, subject to funding, after Snowmass/P5 exercise now under way

- Cost estimate for C^3 250 is $3.7B, plus lab labour and contingency. Many components of this estimate are derived from ILC and CLIC

The Silicon Pixel Tracker

- Assuming ILC or C^3 gets built, we need an excellent tracking system, with minimal material, including the forward region (due to the multi-jet nature of TeV-scale physics)

- ILC Detector Review Panel in 2007 looked at proposals for tracking in Beijng, and we were concerned about all of them. Marcel Demarteau: 'Tracking has always gone to Hell in the forward region'

- By 2008, we had a proposed solution – the Silicon Pixel Tracker, SPT. Konstantin Stefanov, ILC Workshop, Sendai, Japan

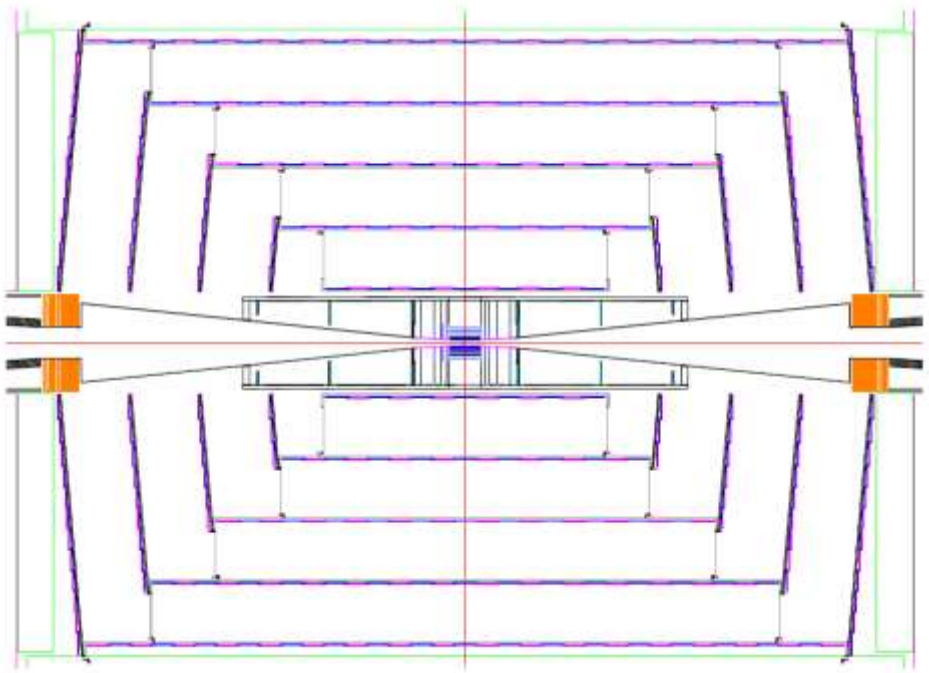
- Immediate reaction was 'It's a case of the better being the enemy of the good! We need to be running by 2020, so we'll stick to the microstrip baseline'

- Over the past decade, the SPT concept has become increasingly attractive, as a result of developments in pixel design (pinned photodiode) and MAPS-based tracking for ALICE (ITS-2, now moving to ITS-3)

- By the time of LCWS-2021, when Konstantin presented an updated conceptual design, it was now considered to be clearly the technology of choice for ILC, at least by the SiD collaboration

- So let's review the design concept (which is also applicable to C^3, though with a different time structure)

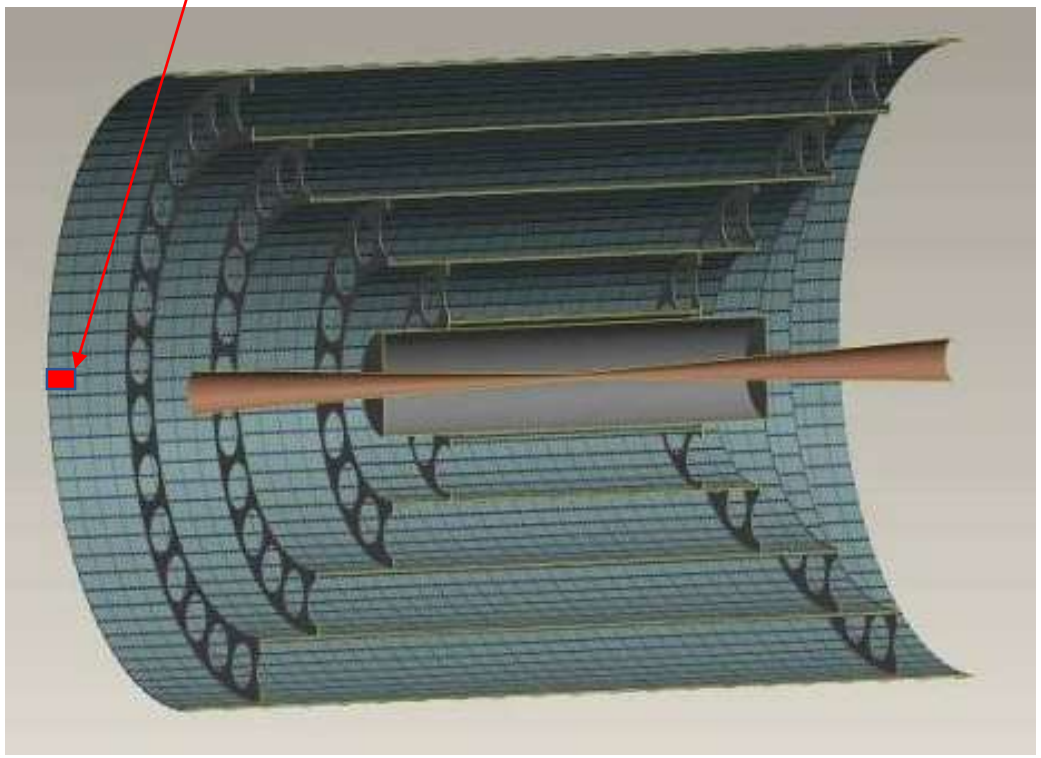
The SiD Microstrip Tracker
(previous baseline)



5 barrels with 4 forward disks at each end (ILC TDR 2013)

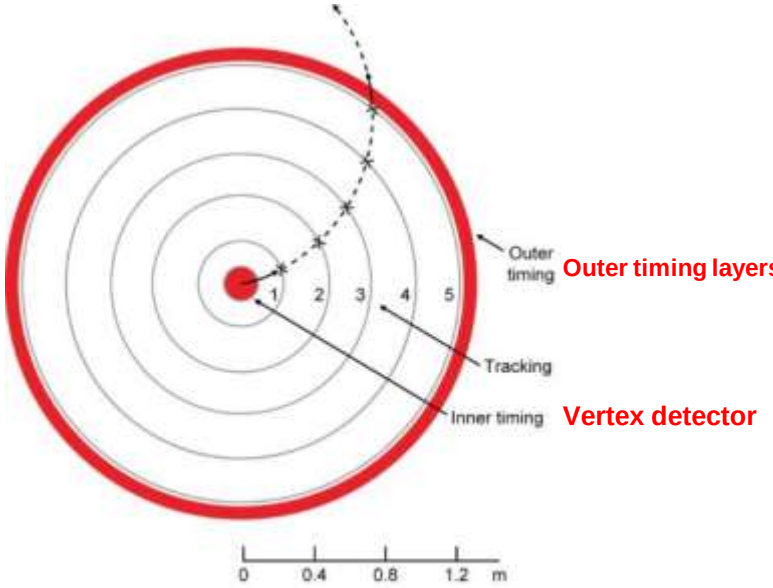
The SiD Silicon Pixel Tracker – SPT (emerging baseline)

Each sensor is a 8x8 cm^2 MAPS of 2.56 Mpixels



Time integrating tracking layers. Endcaps not shown

- Tracking system with high transparency (≈3% X_0) times obliquity factor between 1.0 and 1.41 over full angular range
- Featuring:
  - Low mass tracking layers integrating signals through the bunch train, to minimise power
  - Single bunch timing information from the vertex detector and a dedicated timing layer (just before ECAL) for robust pattern recognition
- A major challenge is to minimise power dissipation, hence material
- Air-cooled, power dissipation in tracking layers ~100 W
- Sensors ≈100 μm thick, low mass support (total≈0.6% X_0 per layer)
- Pixel size around 50 μm × 50 μm, pinned photodiode
- Partly depleted, to deliver ~5 μm measurement precision – we hope! (to be simulated)
- Overall system 28 Gpix, 70 m^2 of silicon
- Square pixels preferred due to equal importance of Rϕ and RZ projections, for some purposes. Another opinion prefers 25x100 μm^2 (both to be simulated)

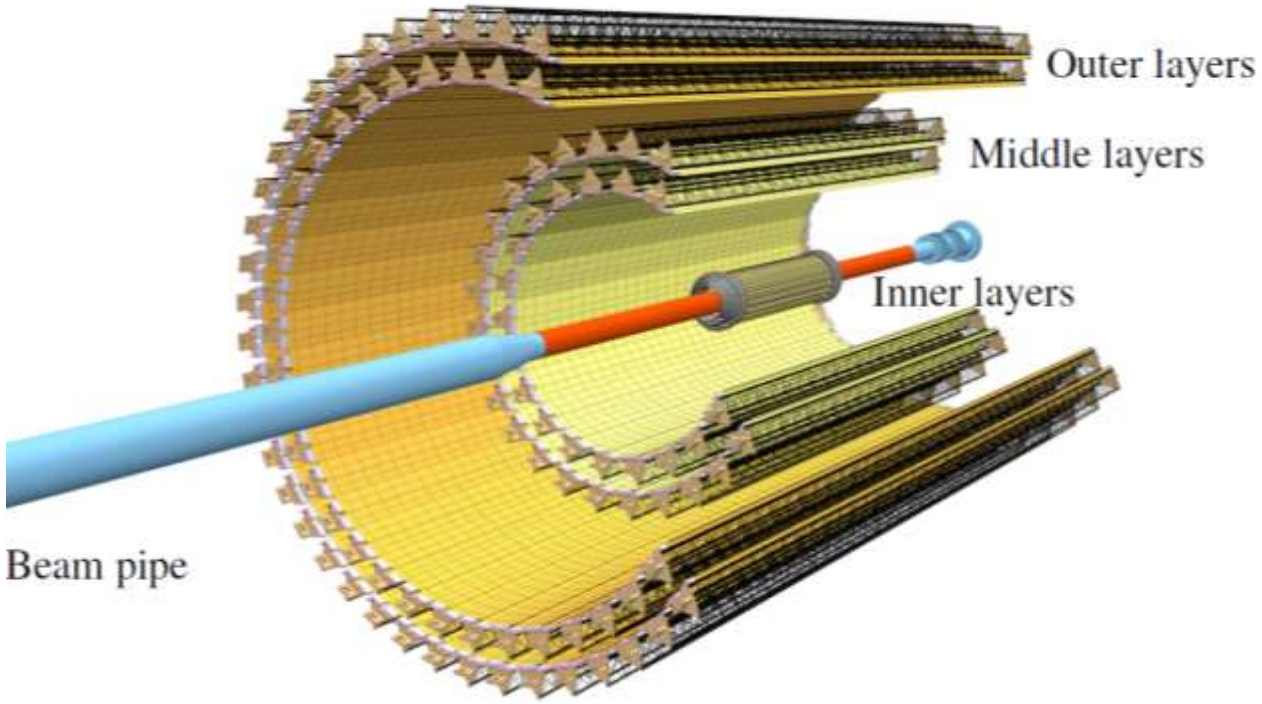


- Outer timing layers (original plan)

  3 closely spaced layers for redundancy
  - Single bunch timing resolution (<554 ns for ILC, ~5 ns for C^3)
  - Material budget less critical due to proximity to ECAL
  - Probably air-cooled
  - 150 µm pixels

- Might now be combined with a RICH-type PID system (mentioned later)
- The vertex detector will provide tracks with single-bunch timing at small radius
- Track reconstruction performance to be simulated and tuned – possibly leading to a more compact tracker
- Breaking news, 9 Feb: we hope to resurrect the SiD tracker simulation by end of March, as part of the Snowmass process (led by Andy White, UTA)

In 2008, we were a bit pioneering, but now we are on firm ground – ITS-2 (ALICE)



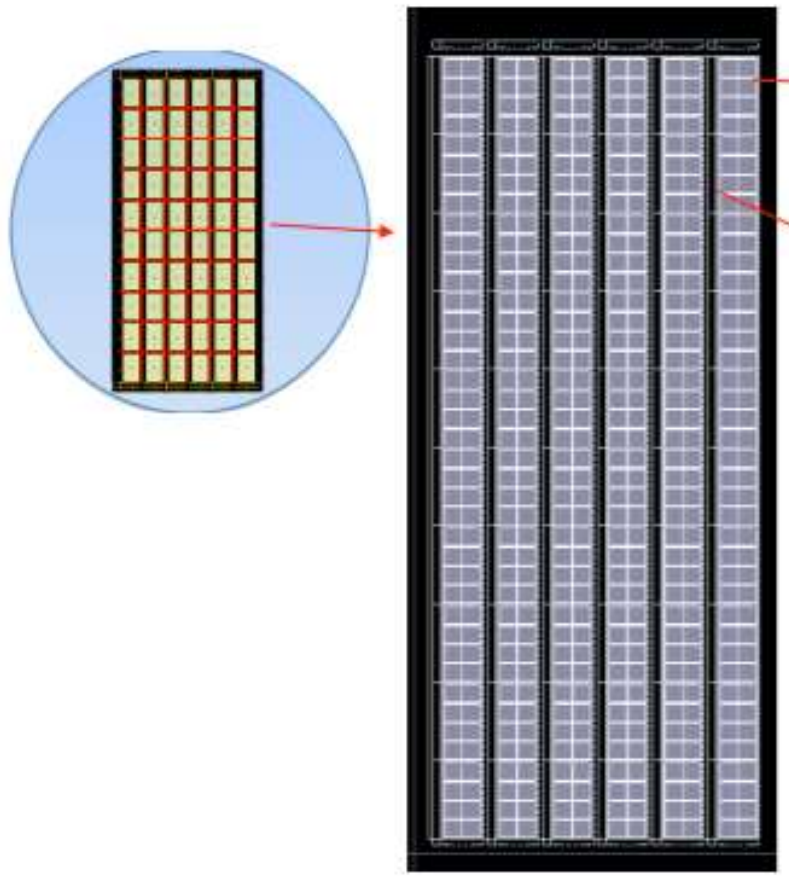
ALICE ITS2 TDR, CERN-LHCC-2013-024

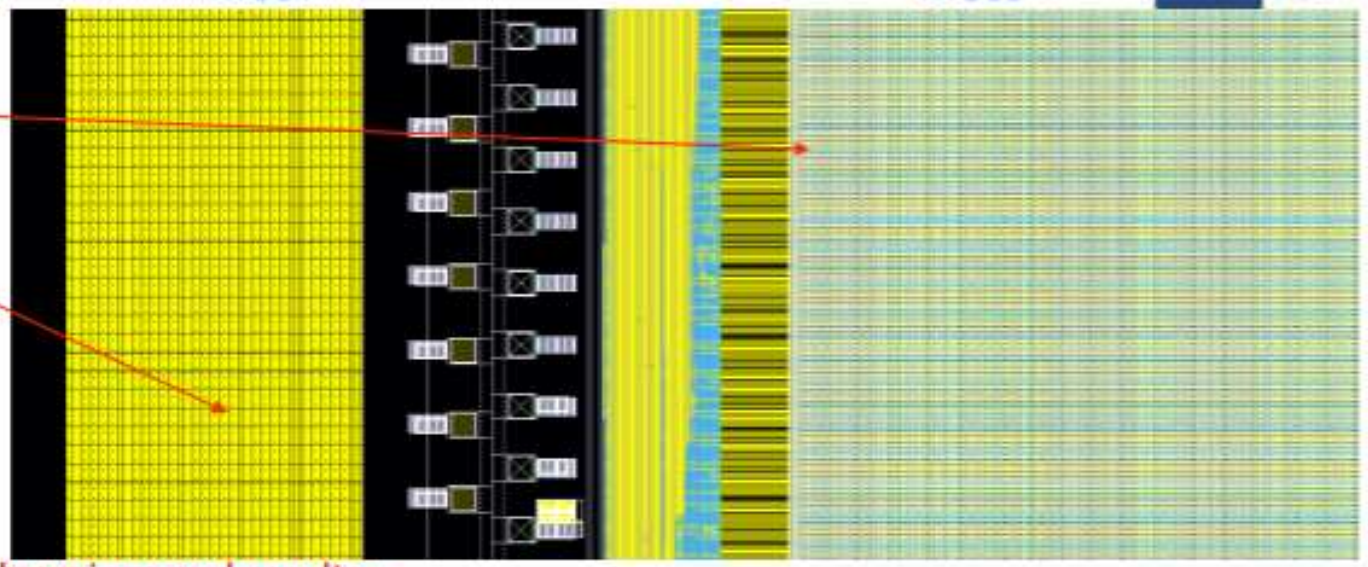
- 12.5 Gpixels
- ≈30×30 µm pixels, ALPIDE MAPS sensors
- Outer barrel 1.48 m long
- Total 10 m^2 silicon (cf 70 m^2 for SiD)

And even more, the work of CERN WP1.2, led by Walter Snoeys, for stitched MAPS devices for ALICE ITS-3 at the TJ 65 nm technology node ….

Pre-mock submission (still on old metal stack)

GDS (final design artifact) begins to appear





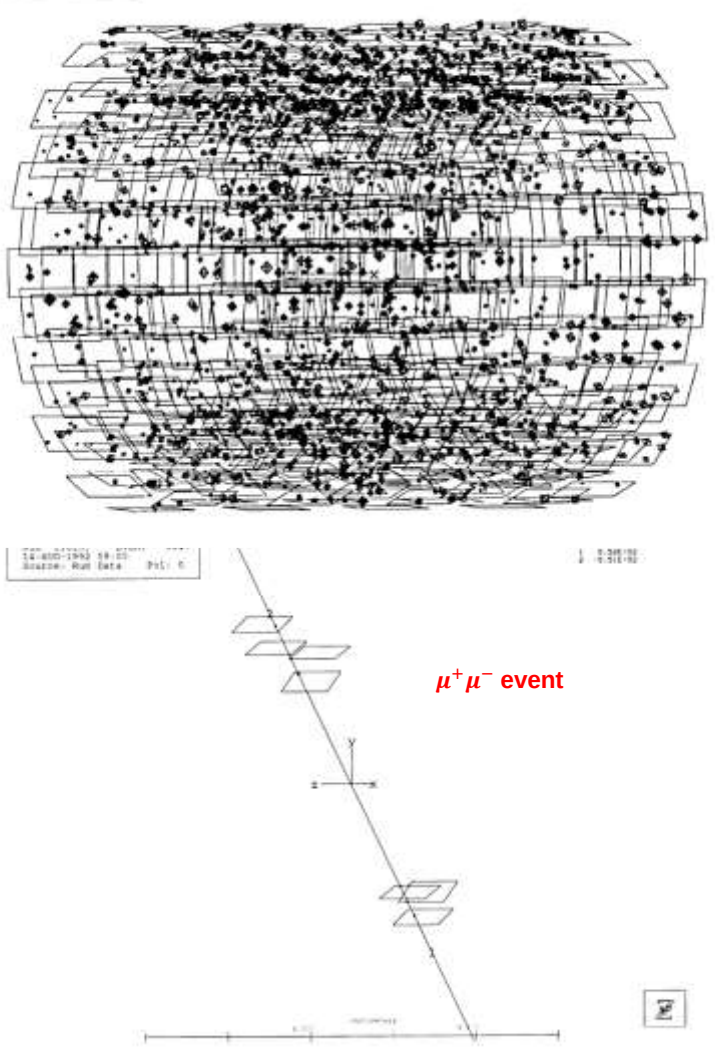
EP R&D

Key learnings and results:

- Valuable experience on procedure for such large gds. DRC on full wafer needed monster machine to complete
- No major issues, floorplan approval confirmed.
- Some clarification of what exactly is printed on the wafer.
- Yield info: significant emphasis on via and contact redundancy, also on overlap of metal over via -> initiated correction of DRC violations of certain recommended rules, prioritized by the foundry for design for manufacturing. (present libraries not optimized for wafer-scale designs)

20220209 | EP RD WP1.2 Report 4

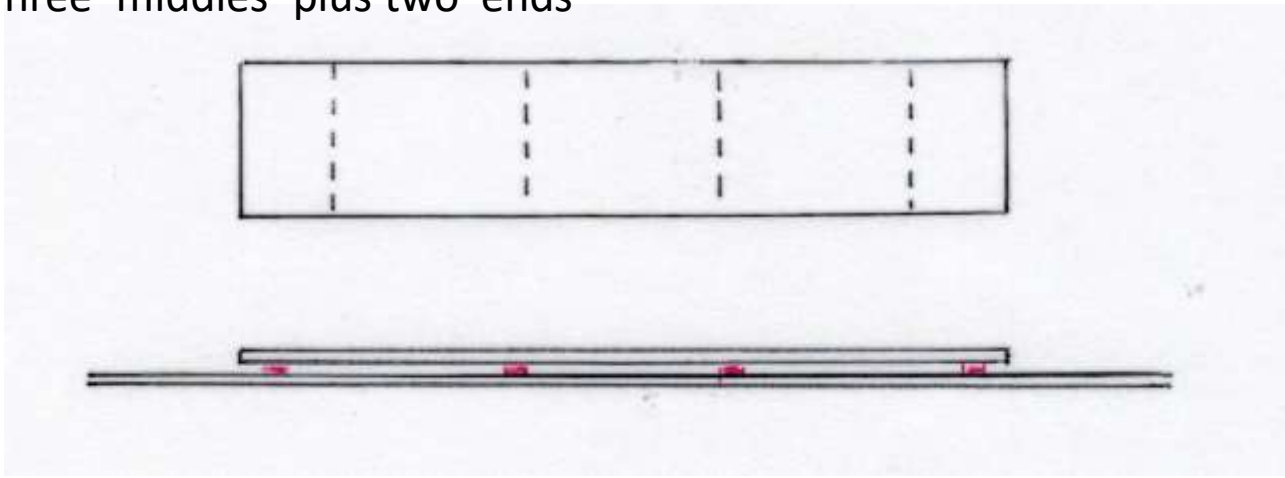
1-D stitching for first submission, each device is 10x2.5 cm by 1.4 cm
Ten ‘middles’ plus two ‘ends’



1990: SLD's VXD2 with 120 Mpixels

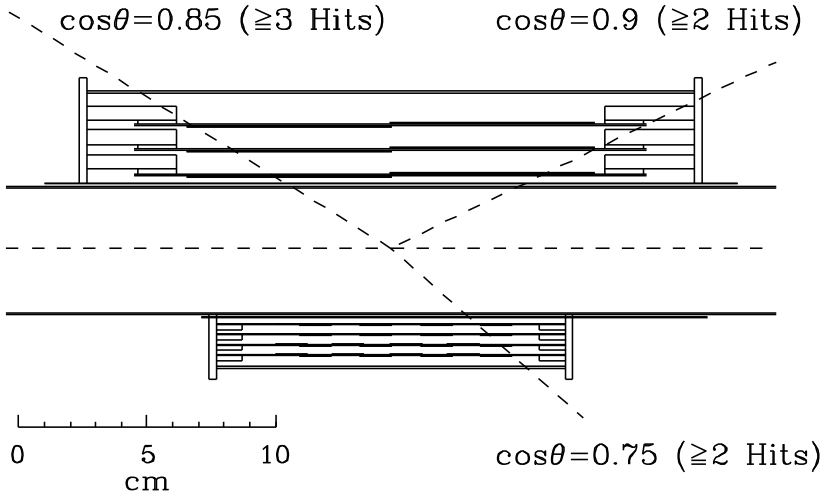
- Low power hence gas cooled, read out over 10 bunches
- Bgd acceptable due to high granularity, in contrast to the Mark II microstrips which 'brought SLC to its knees'

1993: David Burt: thanks to wonderful development of stitching at e2V, we could do a lot better – VXD3 with 307 Mpixels
Three 'middles' plus two 'ends'

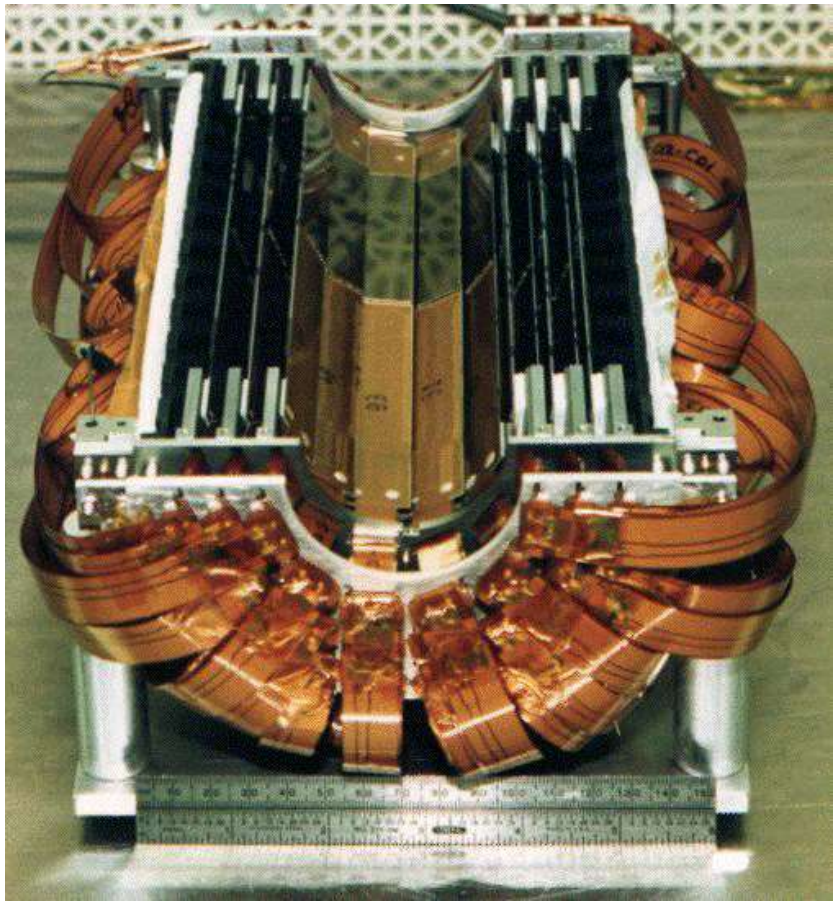


VXD3

R_{bp} = 2.4 cm



VXD2



A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

Eric R. Fossum, *Fellow, IEEE,* and Donald B. Hondongwa, *Student Member, IEEE*

***Abstract*—The pinned photodiode is the primary photodetector structure used in most CCD and CMOS image sensors. This paper reviews the development, physics, and technology of the pinned photodiode.**

***Index Terms*—Charge-coupled device (CCD), CMOS active pixel image sensor (CIS), photodetector, pinned photodiode (PPD), pixel.**

I. Introduction

THE "pinned photodiode" is a photodetector structure used in almost all charge-coupled device (CCD) and CMOS image sensors (CIS) due to its low noise, high quantum efficiency and low dark current. We found that a comprehen-

The photocurrent depends on the wavelength-dependent photon flux $\phi(\lambda)$ incident on the semiconductor and the wavelength-dependent quantum efficiency $\eta(\lambda)$ which accounts for optical reflection, absorption and carrier collection:

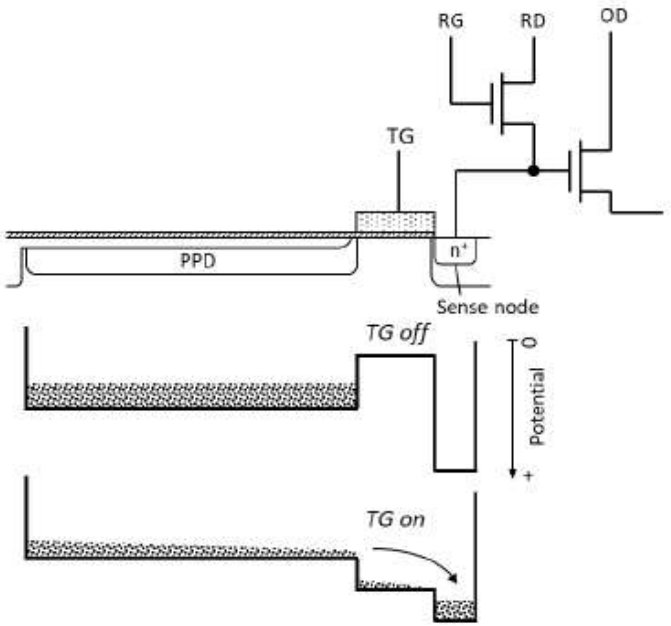
$$I_{ph} = q \int_{\lambda} \phi(\lambda) . \eta(\lambda) \, d\lambda \qquad (2)$$

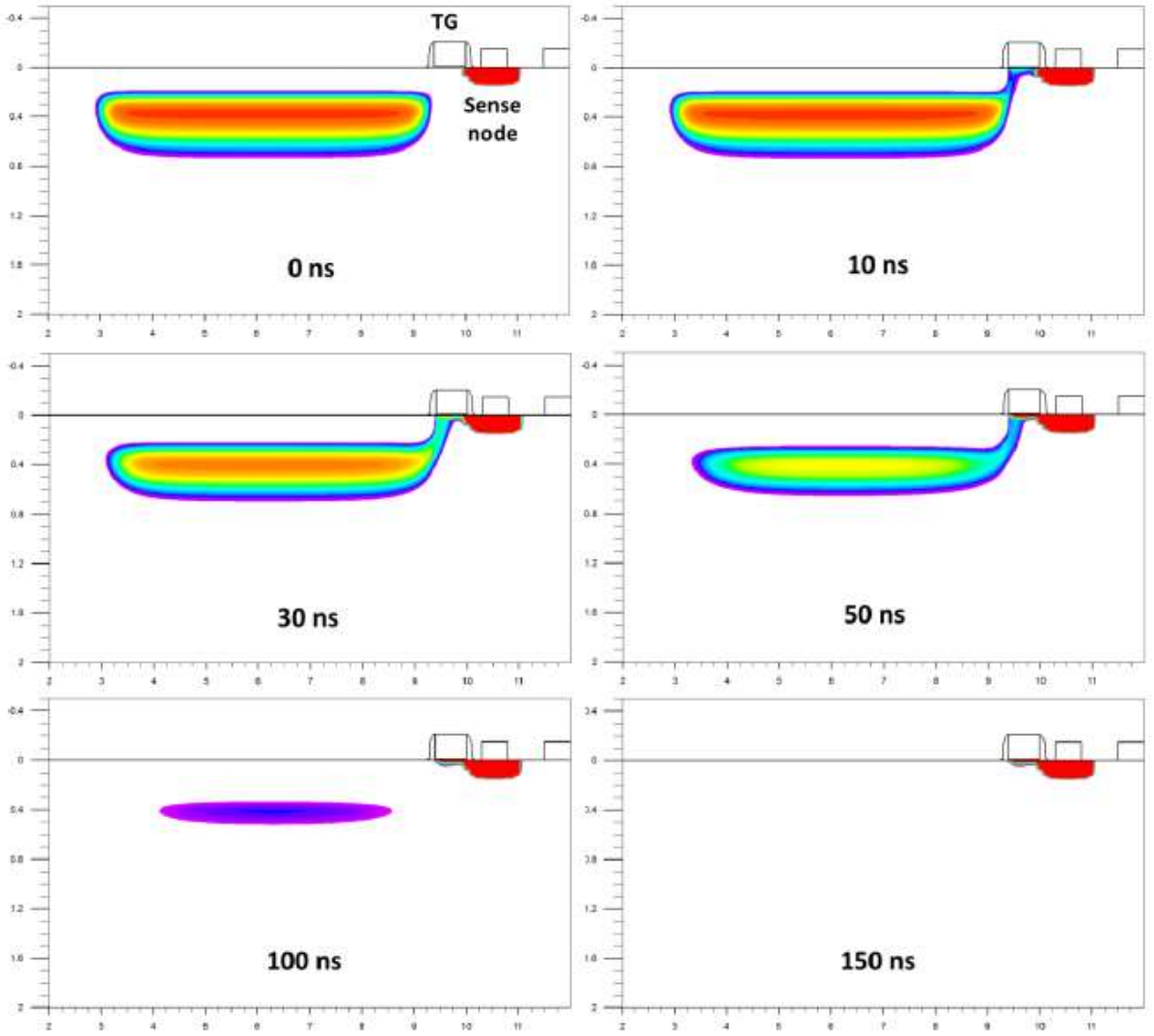
The integrating photodiode was the basis for the earliest MOS passive pixel sensors (PPS) [5].

In 1968, Nobel at Plessey proposed a buried photodiode-structure for MOS PPS to reduce dark current (the collected signal in the dark due to thermal generation and diffusion) and to improve the packing density of pixels [6]. (A more modern-

It's in everyone's phone cameras, yet it's often overlooked by the HEP MAPS community, usually for a good reason …

PPD – charge transfer

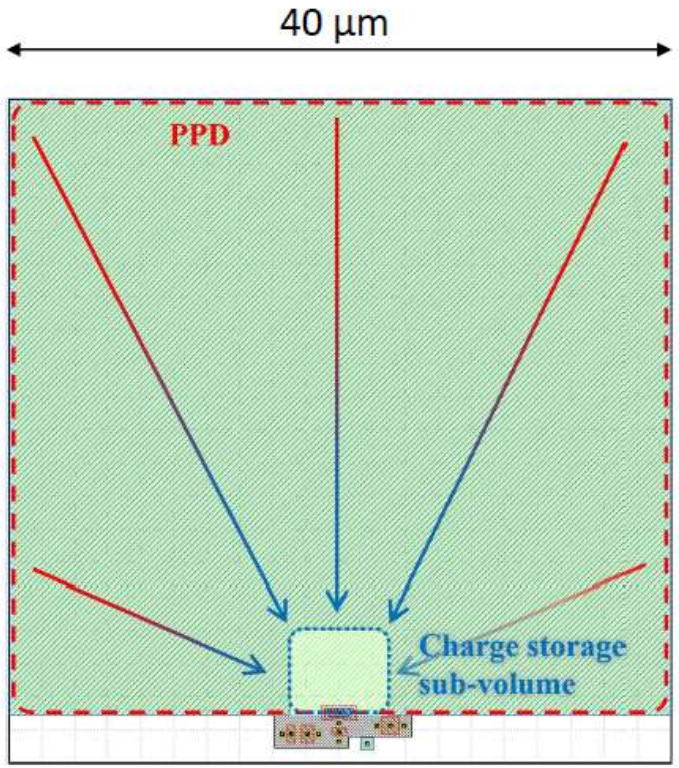




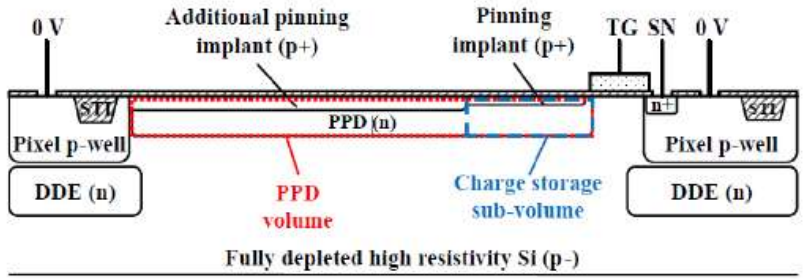
- Combines 3T readout with pinned photodiode
  - Low dark current – few pA/cm^2
  - High conversion gain – separate charge collection and conversion
  - Low noise – sub e- is routine
- Moderate radiation hardness - ~100 krads and ~10^{12} n/cm^2
- Moderate speed
- A very good match for the ILC/C^3 tracker

Meng et al, IEEE TNS 67(6) (2020) doi: 10.1109/TNS.2020.2990081

Large PPD – new development



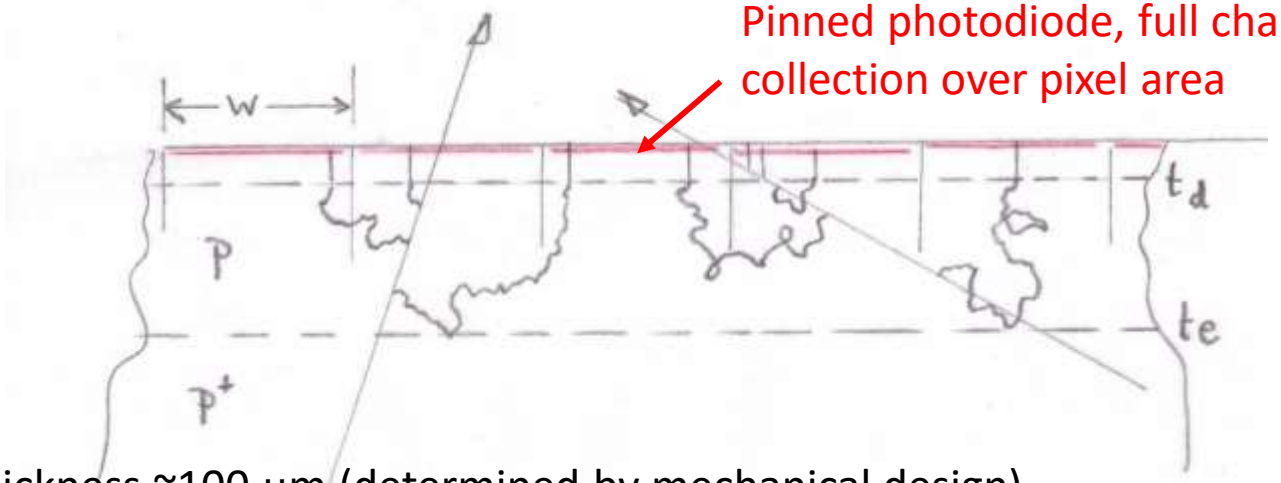
Heymes et. al, Proc SPIE 114540I (2020) doi: 10.1117/12.2560162



- Conventional charge transfer does not work for pixels >10 µm
  - Zero lateral electric field
- Doping gradients have been used to create sufficient field for <100 ns charge transfer
- Here charge diffuses to a 5 µm "sub-volume"
  - Diffusion time is ~1 µs but does not matter, because rows are read out at ~100 ms intervals
- Here fully depleted, needed for soft X-ray applications

Details in Konstantin's slides in Lorenzo Rota's SiD CMOS meeting on Nov 11, 2021
https://indico.slac.stanford.edu/event/7000/

Critical question: can we achieve precision of ~5 μm in track measurement from 50 μm pixels? (since 2008!)



Pinned photodiode, full charge collection over pixel area

Device thickness ~100 μm (determined by mechanical design)
Epi layer thickness t_e ~50 μm (to be optimised)
Depletion depth t_d ~10 μm (to be optimised)

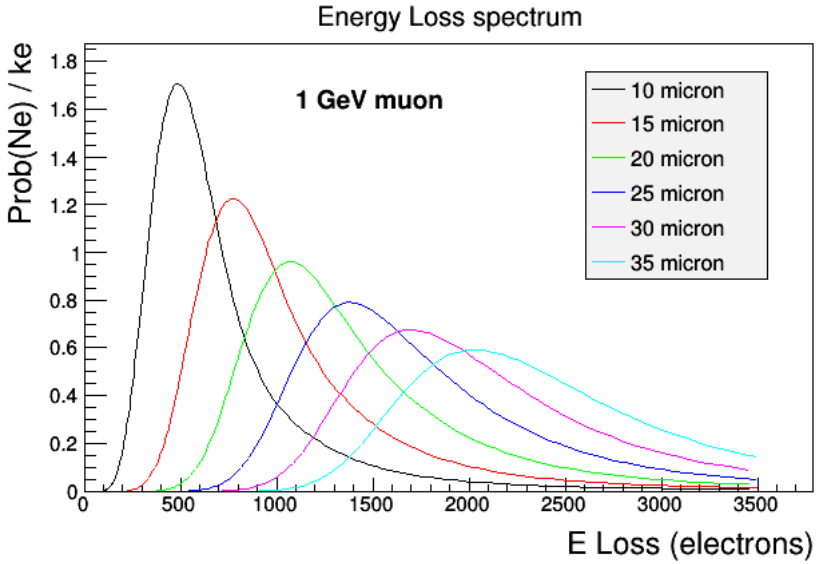
Pixel size w ~ 50 μm square

Vary t_d and t_e to find optimal centroid determination, for incident angles 0 to ~60° wrt to the vertical

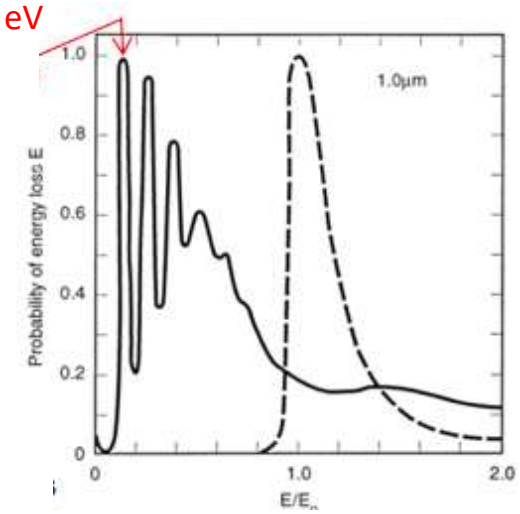
Second phase of simulation will be to study tracking performance with the suggested layout of tracking and timing layers. How compact can it be made? (can probably improve over microstrips)
Valentina Cairo of SLAC is ready to study this

Wonderful News:
Daniel Hynds of Oxford U OPMD, leader of AllPix Squared development, has the tools, and may extend to an experimental test using TimePix4 assemblies

Su Dong, SLAC



Single 17 eV plasmon

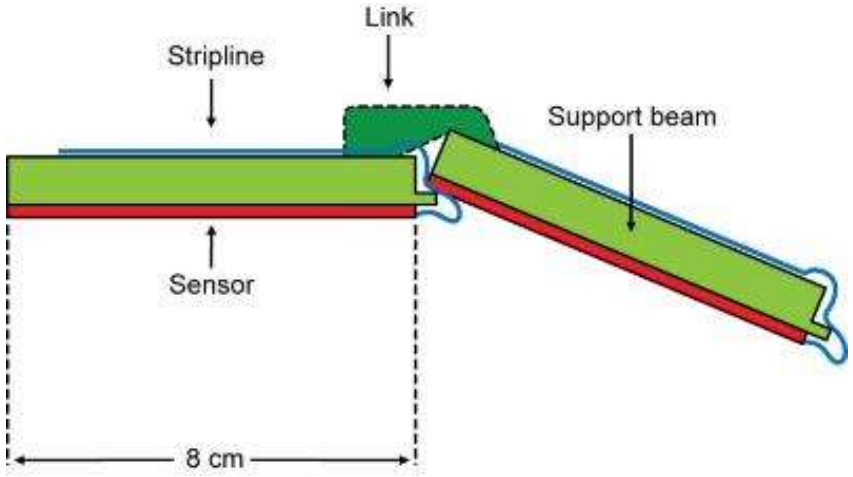


- Hans Bichsel RMP article: primary ionisation process of charged particle traversing silicon is generation of 17 eV plasmons. For very thin layers, the quantised nature of this process is apparent: probability of generating 0, 1, 2, … plasmons, which subsequently de-excite by generation of e-h pairs, heat (thermal phonons) etc. → yielding one e-h pair per 3.6 eV energy loss on average
- These effects are important for oblique incidence (experience with ATLAS pixels – study by Su Dong)

- Readout:
  - Each pixel stores analogue hit information on its sense node
  - The detector is read out in between the bunch trains (simple rolling shutter)
  - Low noise (~10 e-) readout with sparsification
- Digitised (6-bit?) output signal from a 3×3 area round each above-threshold ‘trigger pixel’ to enable cluster centroid fitting
- This also permits one to observe and routinely monitor X-ray backgrounds (this was very informative while running SLD)

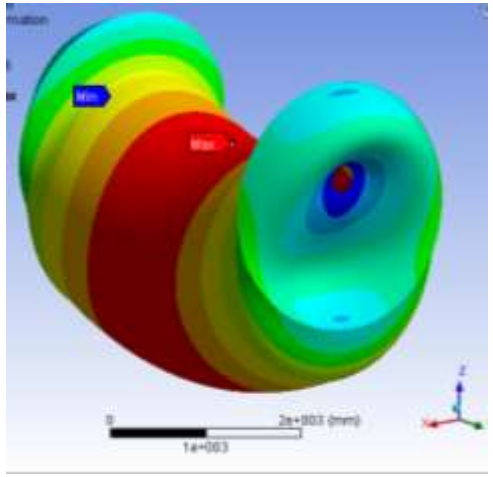
SPT Mechanical Design Concept

- Geometry follows the SiD layout for now, but with quite different construction:
  - Much less material
  - Long ladders made from 4-8% SiC foam (5 mm thick, 0.24-0.48% X_0)
  - SiC is a good thermal match to Si
  - Self-supporting barrel with small foam links at intervals of ~40 cm
  - Structure adhesive-bonded for minimal mass (silicone elastomer, not to be used for high radiation environments)
  - Each half-barrel is attached to its half-endcap for adequate stability during assembly, then the pair of assembled half-barrels are clamped together for full operational stability
  - Combination of optical survey and beam-based alignment completes the process
  - Consistency checks between reconstructed 3-d tracks in the vertex detector and in the main tracker are valuable for fine-tuning track-based alignment of each of them.

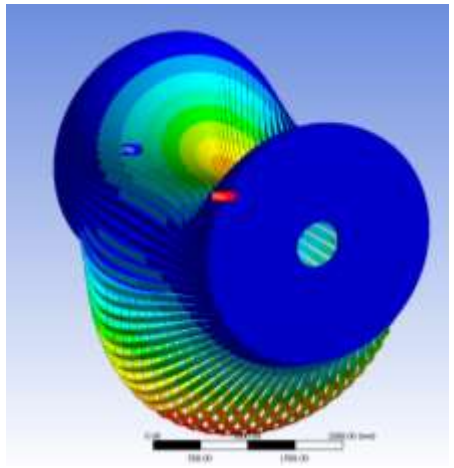


- Support beams run full length of tracker
- Foam links about 1 cm wide at 40 cm intervals

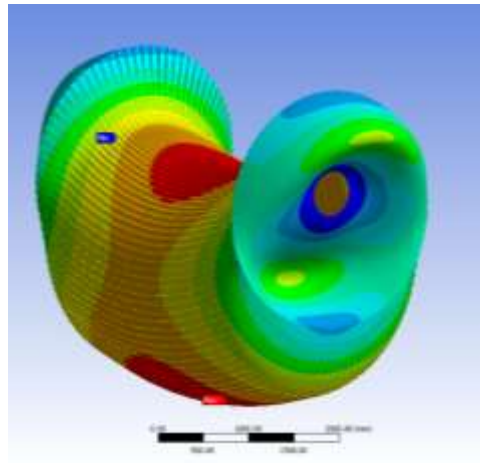
Layer 5



- Continuous foam cylinder
- Max deflection 10 μm



- Separate foam ladders
- Max deflection 20.5 mm



- Ladders joined by small foam piece every 40 cm
- Max deflection 20 μm

Steve Watson - *RAL*

SPT- conclusions and plans

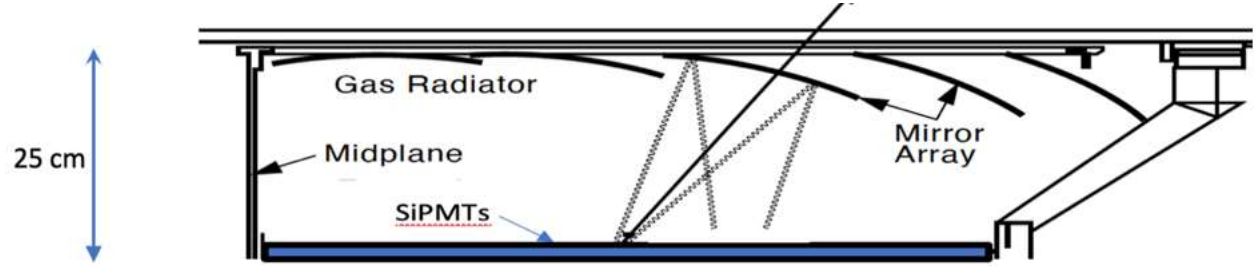
- There's a powerful physics case for a low mass, gas-cooled Silicon Pixel Tracker
- Combining:
  - Highly pixelated barrels and endcaps, time-integrating during the bunch train
  - Single-bunch time stamping for every track from vertex detector and outer timing layers (maybe combined with PID in form of a compact RICH system – work in progress, led by Valentina Cairo and Jerry Vavra, last reported at FCC workshop on 8th Feb)
- Sensors:
  - Widely used MAPS technology (pinned photodiode pixels) appears well matched to the needs
  - Measurement precision of the partly-depleted variant to be checked by simulation and experiment
  - But there's always room for new ideas. On the 15-year timescale, is it possible that the frontier for high performance tracking may have advanced to very rad-hard general purpose stacked devices, which have for some time dominated commercial CMOS Image Sensors (CIS devices)

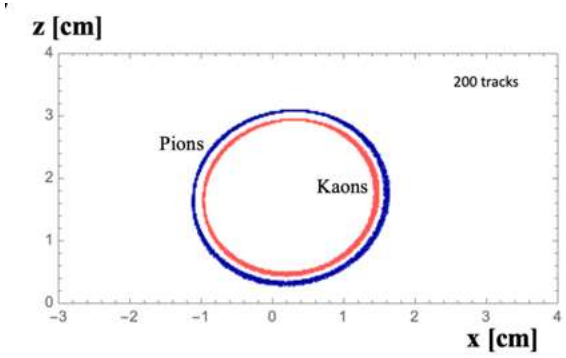
https://cerncourier.com/wp-content/uploads/2021/07/CERNCourier2021JulAug-digitaledition.pdf

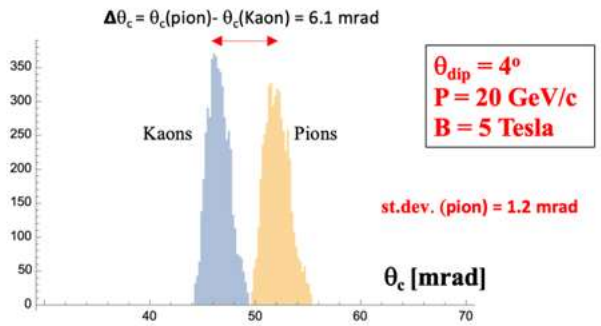
The Strange Quark as a probe for new Physics in the Higgs Sector

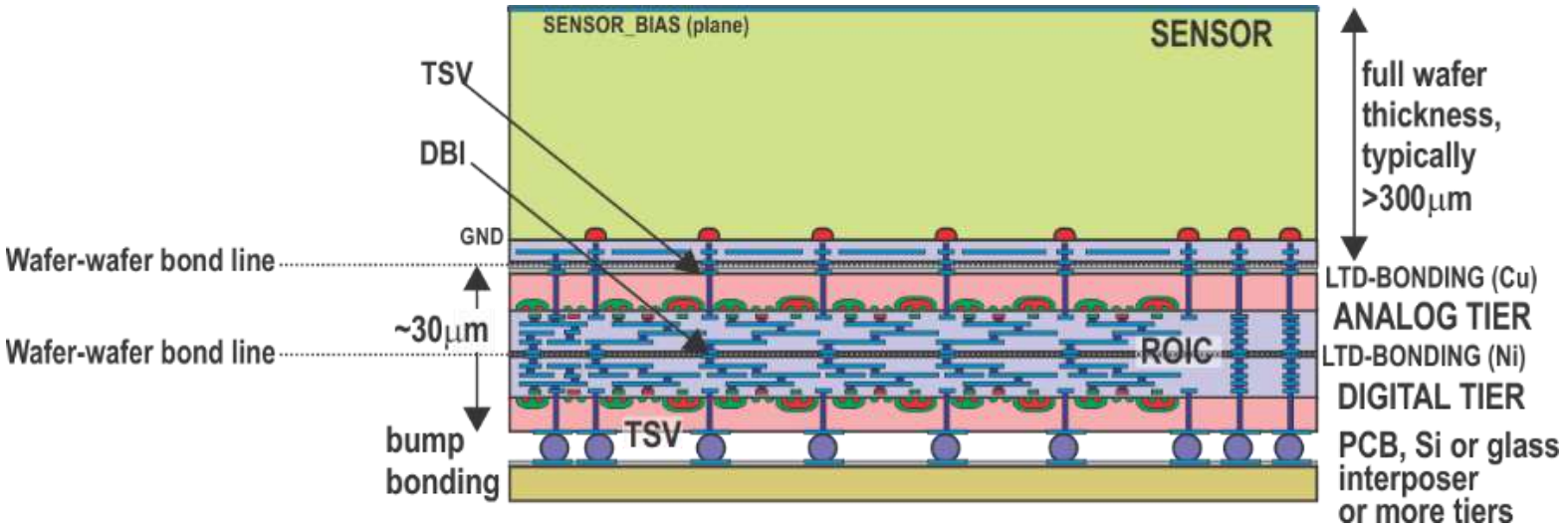
Matt Basso (U. of Toronto)
Valentina Maria Martina Cairo (CERN)
Chris Damerell (RAL)
Markus Elsing (CERN)
Ariel Schwartzman (SLAC)
Su Dong (SLAC)
Jerry Va'vra (SLAC)

- Need K/π discrimination from 8 GeV/c to about 30 GeV/c: beyond reach of TOF, cluster counting, and dE/dx in gas or silicon
- Barrel RICH with appropriate radiator gas (probably $C_4 F_{10}$ at few degrees C), looks promising
- Can be restricted to a thin shell, 25 cm or maybe as little as 10 cm radial space, given further advances in photodetectors
- Material budget, including timing layer functionality, can probably be held below 0.2 X_0
  (needs to be designed, simulated and tested)





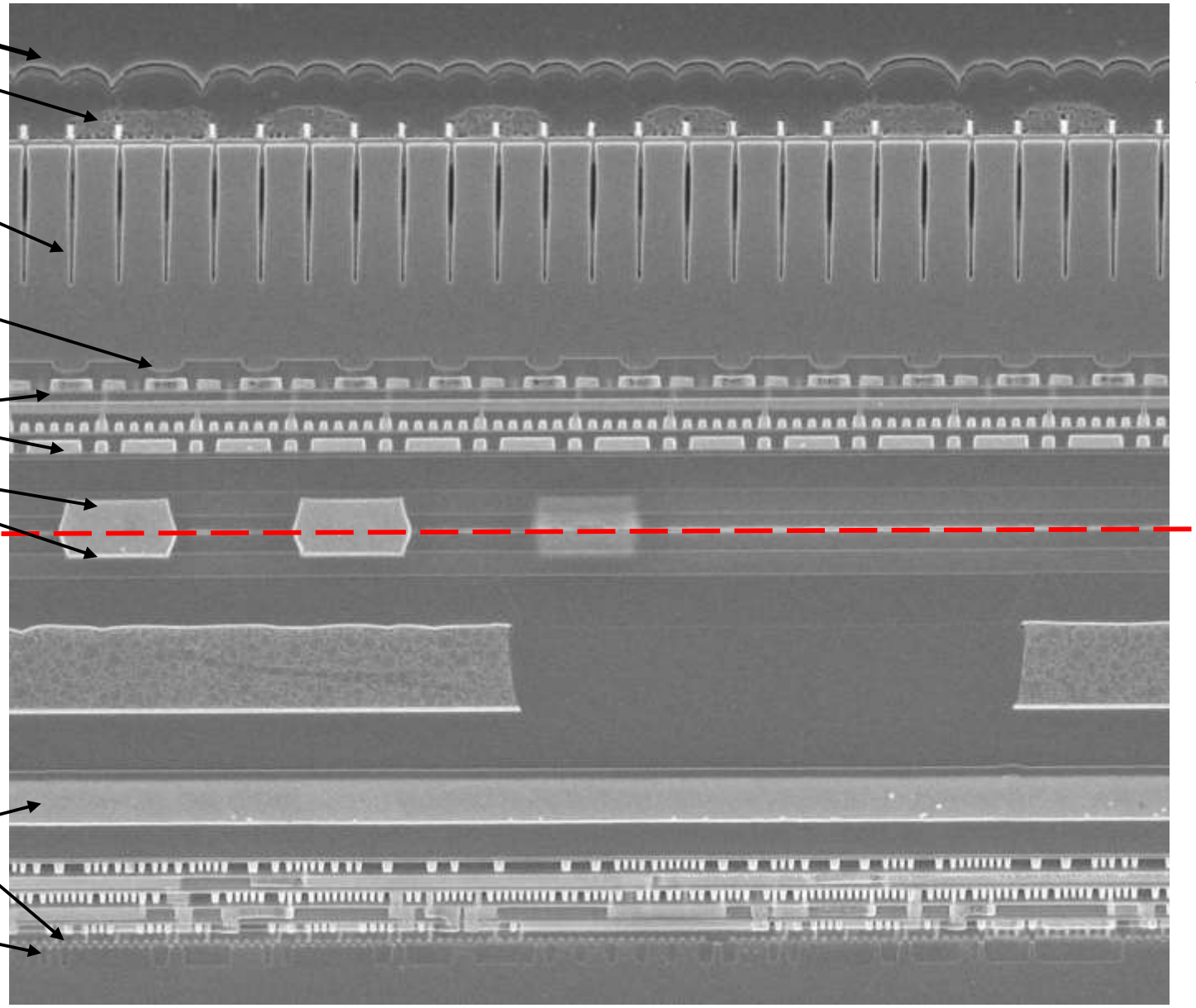




Grzegorz Deptuch BNL

- **Fermilab/BNL stacked pixel detector for X-ray imaging**. Functional sketch, not to scale. 3 layers, comprising a sensor tier (300 μm thick, for efficient X-ray response), an analog tier and a digital signal processing tier (each 15 μm thick). Direct bond interconnects (DBI) and through-silicon vias (TSVs) of dimensions 1 μm x 6 μm provide inter-tier electrical connections.

- Also, an exciting collaboration between SONY and RIKEN (Takaki Hatsui) for advanced X-ray imaging systems. NO public information, but look what SONY are doing for visible light imaging – camera chips.



SONY chip cross-section
Processing and image from Tech Insights

Overall Conclusions

- Maybe our Japanese friends will work a miracle, and get ILC off the ground, with strong Asian, European and North American participation.

- If not, maybe the USA will back C^3, and some other regions will join in.

- In either case, the detector groups have at their disposal exciting ideas for advanced tracking performance, possibly combined with RICH-based particle ID.

- Despite decades of development, weaker options (notably TPCs and drift chambers, still being pursued) are unlikely to succeed. Just my opinion

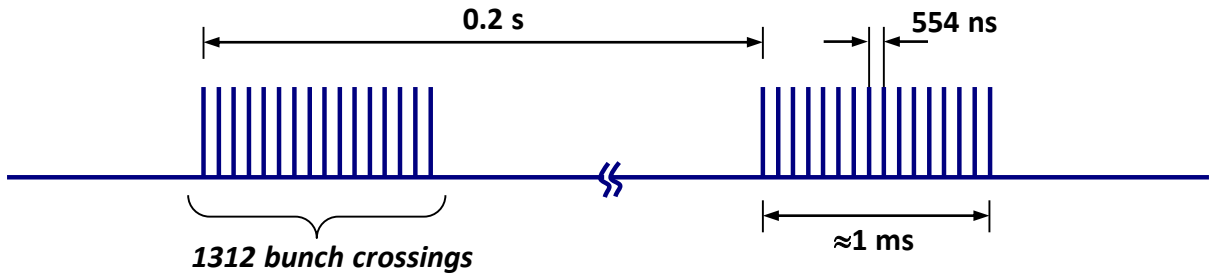
- Whatever happens, there are some basic truths:
  - the energy frontier won't go away
  - circular colliders can't get there
  - at the TeV scale one absolutely needs minimal material in the tracker over the full angular range
  - A PID system for s-jet identification may be a game-changer for BSM physics

- 'Nature cannot be fooled'.

MIT Engineers Create the “Impossible” –
New Material That Is Stronger Than Steel
and As Light as Plastic
MIT Technology Review 27 Oct 2021

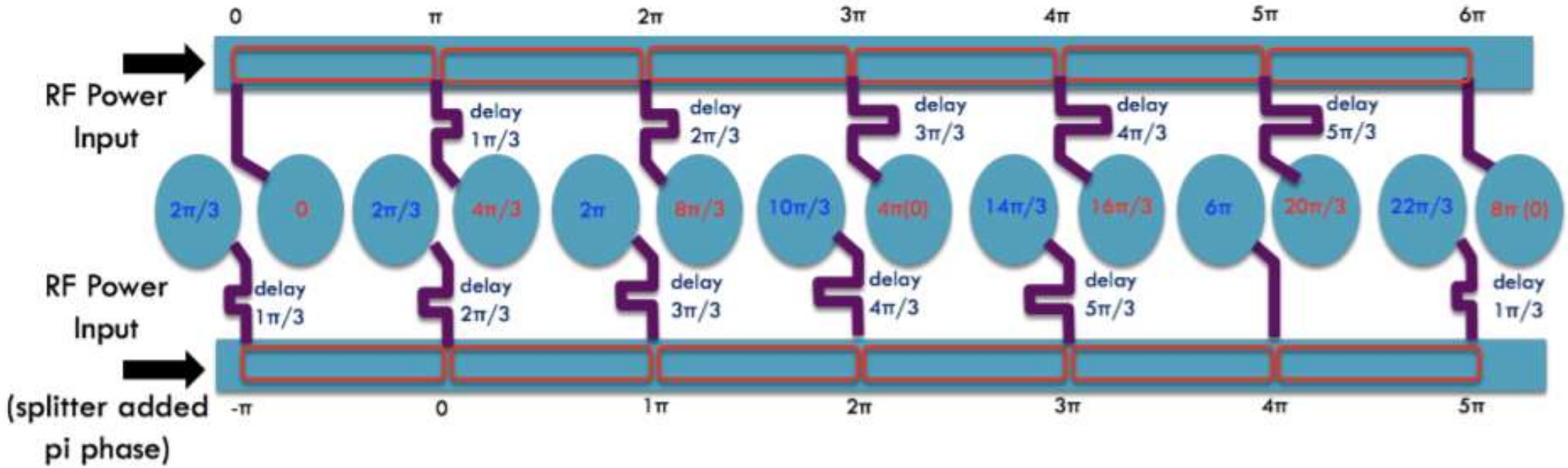
backup

Bunch structure at the ILC 250 GeV



C^3 at 250 GeV has trains of 133 bunches, spaced at 5.26 ns, at train repetition rate of 120 Hz

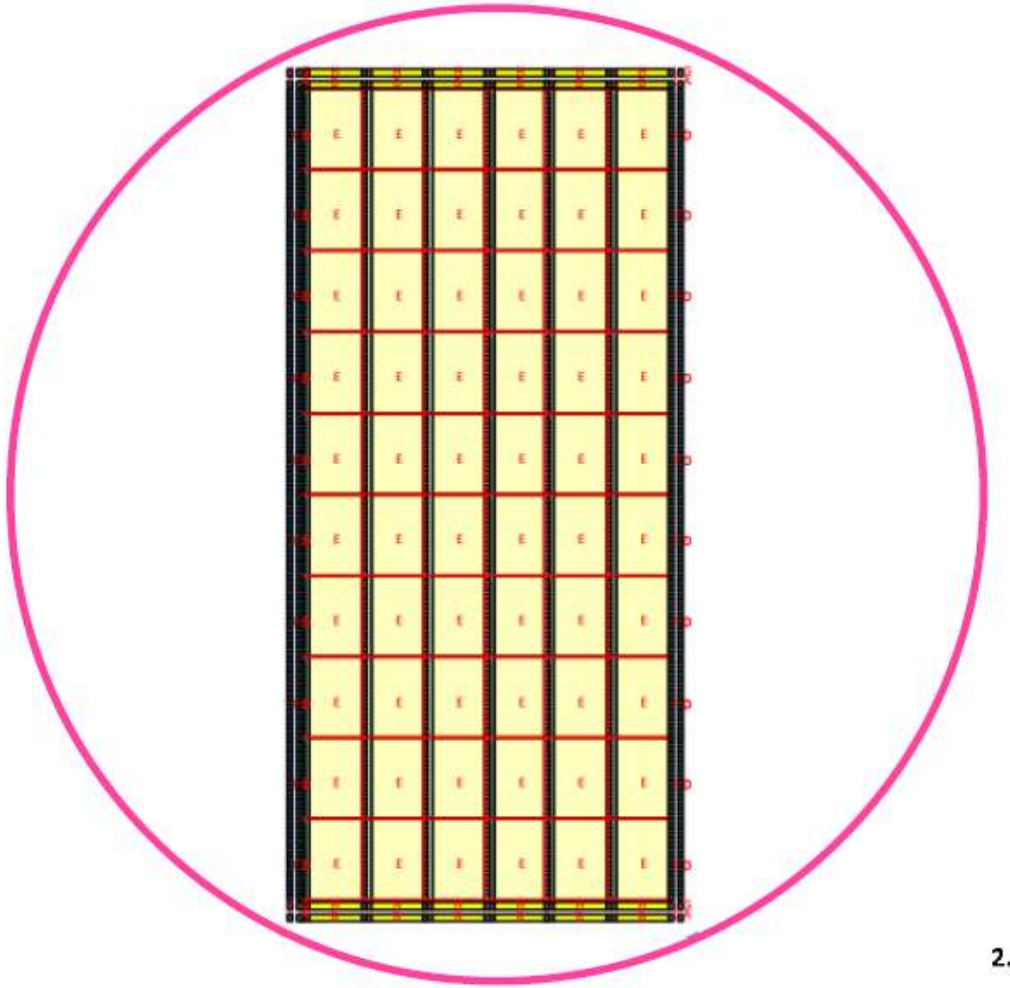
This factor in train rate means that the tracking layers are 24 times cleaner than at ILC.
All needs full simulation, but we are pretty confident for both.



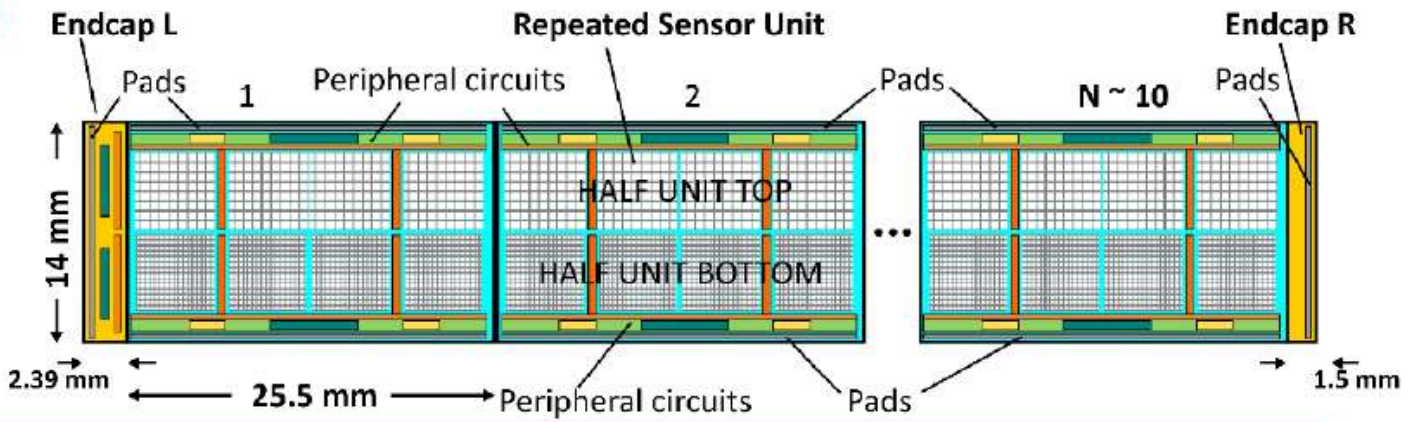
Variant with 120 degrees phase advance per cell
Optimal (from simulation) would be 135 degrees
Currently, π-mode, so $0, 180, 360, 540, \ldots$

Towards a wafer-scale sensor

ER1

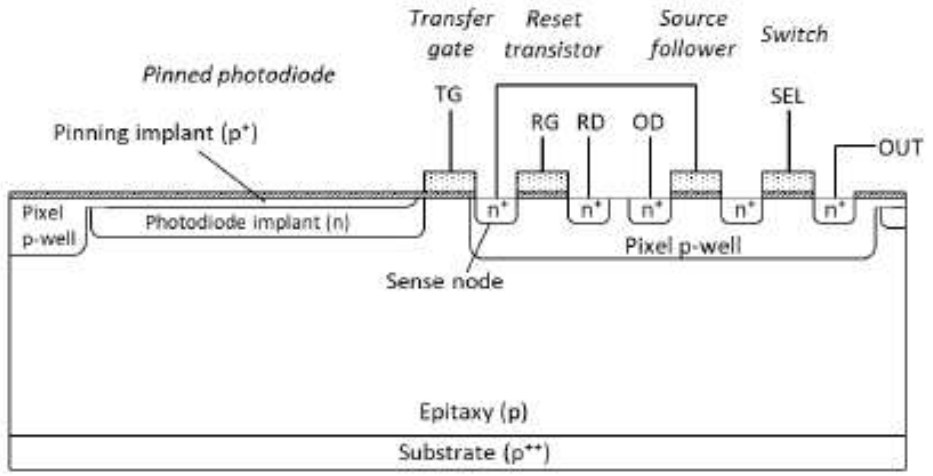


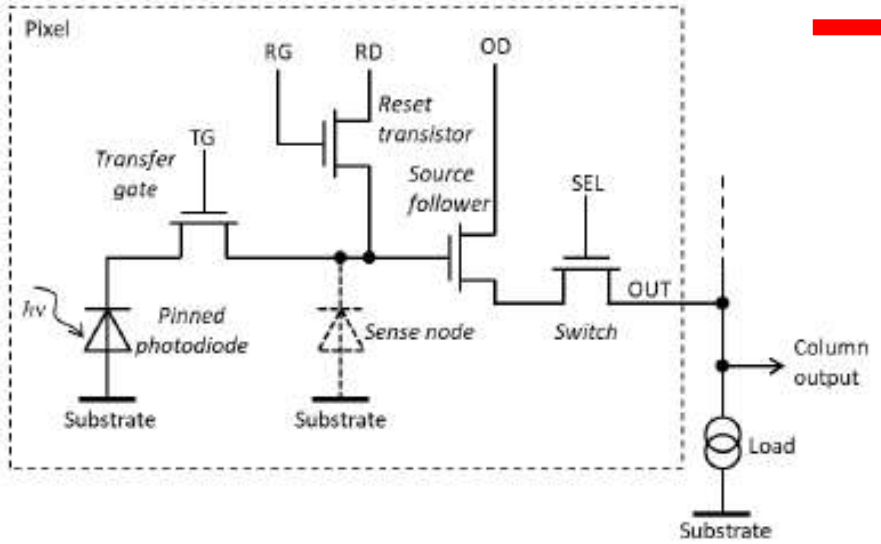
- Next big milestone in sensor design: **stitching**
- Design activity at full swing
  - building blocks are defined and work is distributed
  - builds on very encouraging, **silicon-proven**, feedback from MLR1
  - floorplan under discussion with foundry
- Plan (without contingency):
  - for mock submission: end 2021
  - final submission: Q1 2022



Last crucial ingredient for the TDR

Pinned photodiode – overview





- Used in most CMOS image sensors
- Combines 3T readout with a pinned photodiode
  - Single charge transfer
  - Low dark current – few pA/cm^2
  - High conversion gain – charge collection and conversion are separate
  - Low noise, sub 1 e- is routine
- Moderate radiation hardness
- Moderate speed
- A good match for the Silicon Pixel Tracker?