# Probing extreme-energy universe with EeV neutrino detection

Improving Radio Frequency Detectors with Programmable Logic at ANITA and PUEO

C. Xie University College London







PAYLOAD FOR ULTRAHIGH ENERGY OBSERVATIONS

RF integrated Programmable Logic (RADIO FREQUENCY SYSTEM-ON-CHIP)

Produced by cosmological particle accelerators that are sources of most energetic particles known (ultra high energy cosmic rays)

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Active Galactic Nucleus in galaxy M87

GRB 151027B

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> >100 TeV CoM energy (vs. 13 TeV at LHC)





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arXiv 1903.04333

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Antarctic Impulsive Transient Antenna

Long duration balloon payload

### ANITA payload



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- Neutrino detection primarily from coherent RF emission from neutrino interactions with ice

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# ≜UC.

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- Satellite interference

### ANITA payload







### **PUEO** overview

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Next generation: Payload for Ultrahigh Energy Observations







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216 antennas (vs. 48 on ANITA-IV) + Programmable Hardware (RFSoC)





PUEO

4x more antennas

# <sup>A</sup>UC

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PUEO



Programmable hardware

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Beamforming trigger combines signals from antennas to lower threshold



PUEO





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# <sup>A</sup>UC

## **PUEO** overview

Next generation: Payload for Ultrahigh Energy Observations

216 antennas (vs. 48 on ANITA-IV) + Programmable Hardware (RFSoC)

- Beamforming trigger combines signals from antennas to lower threshold
- Additional benefits
  - Real time digital filtering of radio interference
  - Improved pointing resolution



PUEO





Programmable hardware

Detecting ultrahigh energy neutrinos with RFSoCs

# 

### Beamforming – why and how?

### N Antenna Sum



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→ Lowers trigger threshold, improving detector sensitivity



### <u>N Antenna Sum</u>

Geometry requires 'delay and sum'



→ Lowers trigger threshold, improving detector sensitivity


### N Antenna Sum Geom

Geometry requires 'delay and sum'



→ Multiple beams required for different sources locations

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Digitisation combines functionality of many analogue components

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### ANITA analogue trigger



Digitisation combines functionality of many analogue components

#### Front-end Amplification cPCI Crate Instrument Box 1200 MHz lownass 35 dB LNA Square-Law Detector + beamforming diod (identical to VPol) LCPol HPol HPol - RCPol 20 ft SFX-500 Second-Stage Amplification 3 dB 45 dB attenuator LNA Flight Computer < 🔸 GPS Antennas, NASA SIP, Sun Sensors, etc. Disk Storage (Helium Drives)

## ANITA analogue trigger

PUEO digital trigger with RFSoC

## Why digital beamforming with RFSoC...

Digitisation combines functionality of many analogue components



## ANITA analogue trigger

Digitisation combines functionality of many analogue components



## ANITA analogue trigger

### PUEO digital trigger with RFSoC



RADIO FREQUENCY SYSTEM-ON-CHIP

- High computational power: FPGA with 4000+ digital signal processing slices
- Natively multichannel
- High fidelity:12-14 bit
- High frequency: 4-6 GHz

Digitisation combines functionality of many analogue components



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XILINX. ZYNQ

GEN 1

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- ✓ Low power

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## ANITA analogue trigger

✓ Increased computational capacity

- ✓ Low power
- ✓ Reconfigure In-flight

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threshold vs. ANITA



0.0

6

3

Peak Single-Antenna SNR

4

(m) -1 1

2 3 -3



Detecting ultrahigh energy neutrinos with RFSoCs

arXiv 2010.02892



Detecting ultrahigh energy neutrinos with RFSoCs

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Detecting ultrahigh energy neutrinos with RFSoCs

Beamforming prototype



### Beamforming prototype

Programmable logic

Manufacturer tools + hardware description language



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Manufacturer tools + hardware description language

Software for on-board CPU

Program clocks + generate simulated signal/noise



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### Improved signal to noise ratio

Demonstrated beamforming improvement for trigger threshold



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Demonstrated beamforming improvement for trigger threshold



Cross-Channel alignment achieved

Phase jitter under 0.01ns  $\ll 0.33$ ns sample period



Result: shown hardware capable of beamforming

## I. Demonstrate on hardware

Manufacturer tools + hardware description language

Program clocks + generate simulated signal/noise

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# Resource utilisation\*

Full 12 bits	Reduction to 5 bits
Inefficient addition	Carry-Save addition
50-100% Cannot be implemented	<10%

\*8 channels and 8 samples per clock cycle Limited by either DSP (Digital Signal Processing) blocks or CLB (Configurable Logic Blocks) As % of available resources on Xilinx ZU28DR device

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#### Bit reduction

Trigger efficiency with bit reduction (at SNR=1.6)



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Result: demonstrated techniques for adequate computational resources for beamforming

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ANITA-III flight snapshot



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Interference reduces trigger sensitivity

Power Spectral Density (dBm/MHz) 25 20 15 Satellite interference 10 5 Frequency (MHz) 0 200 400 600 800 1000 arxiv 1709.04536

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- Impact also dependent on field of view





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Want <u>tuneable filters</u> – can programmable logic help again?





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Utilisation	Width to -10dB
10%	230MHz
20%	60MHz
40%	15MHz



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Centre of stopband tuneable with simple change to filter coefficients

# Result: tuneable digital filter possible but requires significant resources and implementation effort



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### ANITA's signatures



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- Low power





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Flight scheduled for 2024





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Expect neutrino detection from several cosmogenic models





