Commissioning of L1Calo phase I upgrade at ATLAS: development and testing of the eFEX

IOP HEP

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Intro

- I'm Gareth

- I work on software and firmware development for the ATLAS L1Calo Phase I upgrade

- Today I'm going to
  1. Explain what this means
  2. What this means day to day
  3. What physical work actually goes on
  4. What's next as the LHC turns on

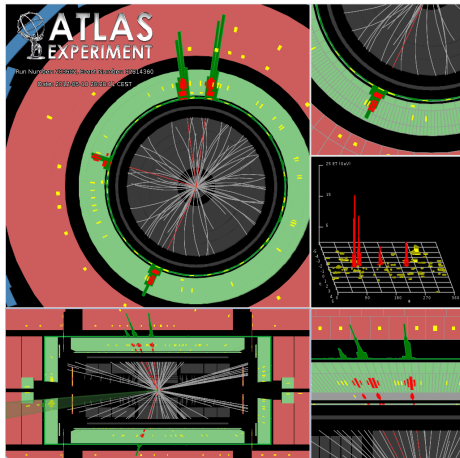- Mostly talking from a UK perspective on a global experiment

Part I

ATLAS L1Calo Phase I Upgrade for dummies

What is ATLAS
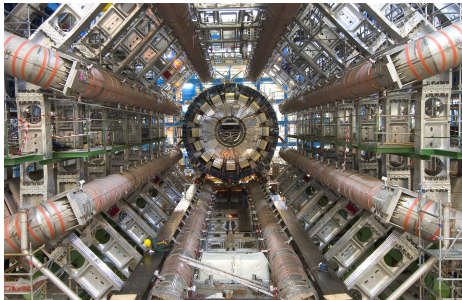
What is L1Calo?

In brief:

- ATLAS can't store every event, 2.5 μs decision deadline

- L1Calo is a hardware trigger that identifies calorimeter based physics objects (e.g. jets, missing E_T, e/γ, τ)

- This reduces the event rate (40 MHz to 100 kHz) which is passed to the software based HLT (High Level Trigger) and provides Regions Of Interest

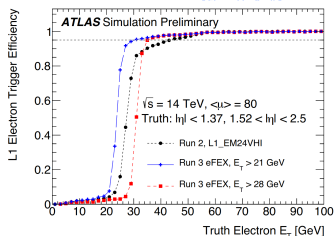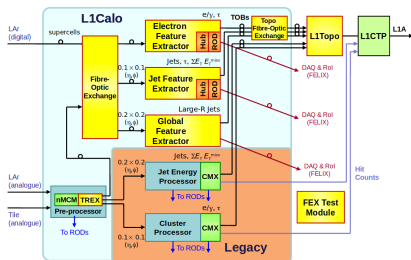- The system utilises high-speed, fixed-latency FPGAs (Field Programmable Gate Arrays)
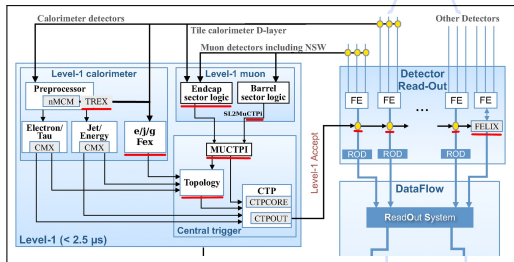
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3 Collaboration ATLAS. "Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System". In: (2013). URL: https://cds.cern.ch/record/1602235

What/Why Phase I upgrade

A new menu of trigger thresholds will be implemented by 3 new Feature EXtractor modules (FEX). This involves a whole new suite of modern hardware.

- Technology has improved since 2008
- New boards are required to process additional granularity and also improve algorithmic capability.
- The new outputs are topologically combined
- The system used in Run 1 and 2 will become legacy: the 'known system' when ATLAS is turned back on

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[4] Collaboration ATLAS. *Performance studies of the ATLAS L1Calorimeter trigger upgrade for run 3.* Tech. rep. Geneva: CERN, 2018. URL: https://cds.cern.ch/record/2309479

The UK Hardware: eFEX

- electron Feature EXtractor (eFEX), generates e/γ and τ candidates using 0.025x0.1 (η, ϕ) input granularity from LAr with improved isolation variables compared to the 0.1x0.1 e/γ module in Runs 1 & 2
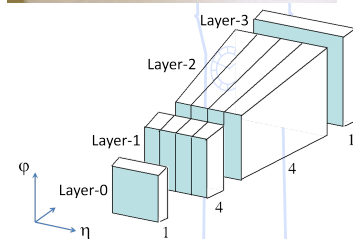
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[5] Collaboration ATLAS. "Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System". In: (2013). URL: https://cds.cern.ch/record/1602235

Test Rigs

- Initial testing of electronics, optical connections, firmware is done at the respective home institutes
- These boards are shared between institutes for further testing
- In the last year a large amount of tests have been done to test interconnectivity nationally and at CERN. Notably Slice Tests!
  - ▶ STF: The underground Surface Test Facility used as a shared space between institutes to do this
  - ▶ Group work organised into 'Slice Weeks' aim to reach specific targets of connectivity and functionality
- All these tests will develop and continue!
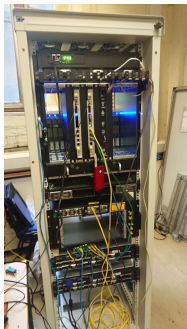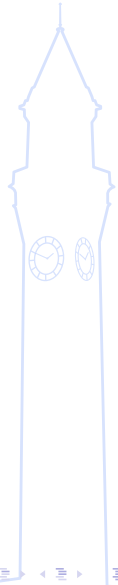

Birmingham

CERN USA15 @ P1
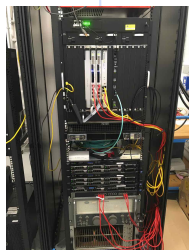
RAL

Cambridge
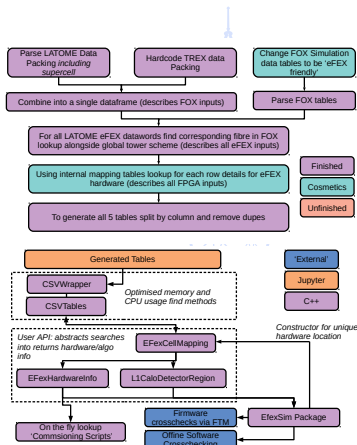
Part II

What my work entails

An Example Job: LATOME Align Frame Readout Tests

Fancy Words For Checking Things Are Plugged Right: 130k data words arrive at the eFEX on 4.7k inputs!

- Breaking down the words
    1. **LATOME** LAr's Phase I upgrade digitizer boards for the trigger
    2. **Align Frame** A data packet sent by a LATOME that tells us what fibre and LATOME board we are being sent data from
    3. **Readout Tests** Going through the readout path to check is what we receive matches expectation (eFEX raw output)
    4. **Online Software** Configures, calibrates and runs boards at test rigs and the real system. Contains bitwise simulation of the boards for these purposes.

- My job is to write the online infrastructure to generate a program that checks connectivity of new eFEXs as they arrive at P1 and gives meaningful debugging info by combining hardware readings to simulation

Writing Software

Science and Technology Facilities Council

- The flow: send L1As to eFEX that are connected to LATOMEs on Align frames (BC 0xDAC)

- channelMappings Underneath layers of simulation of my understanding of LATOME,FOX and eFEX cabling down to dataword level (right)

- hubControl pulsing one L1A to capture the right data

- efexTests Combining many parts together into a final script

- These work, things are plugged in right!
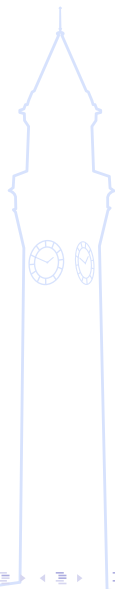
Part III

Assorted Racks, Modules and Cables

The day to day at CERN
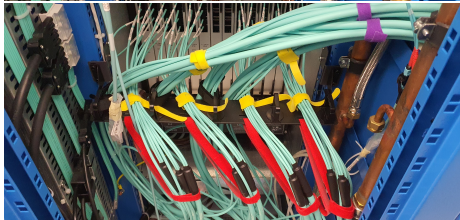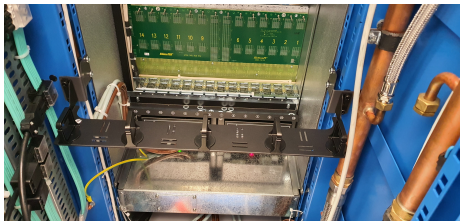
- Tidy cable organsiation of two(ish) shelves
- Movement of many eFEX
- ~ 30 HLT Servers
- Running STF and P1 software for tests

Part IV

Beams and the final crunch

2022: The finale

- The absolute deadline for ATLAS is being ready for stable beams and physics
- Intentionally haven't mentioned the difficulty acquiring eFEXs and the silicon shortage
- Essential that lots of working parts of the system are ready for beam in the order of weeks
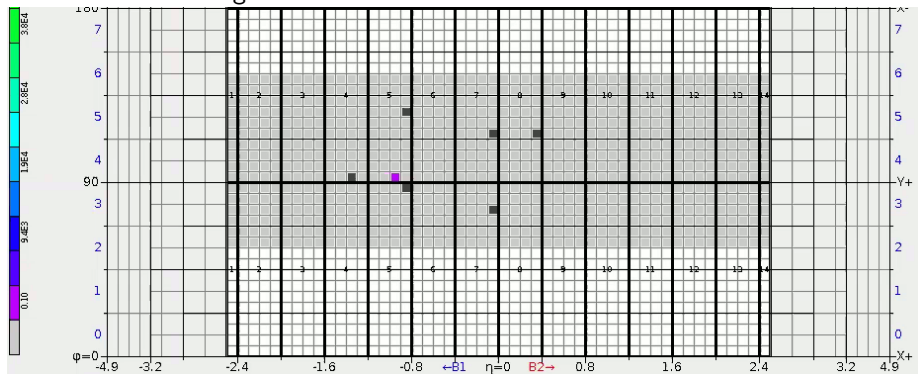- The work then doesn't stop, continuous monitoring and calibration
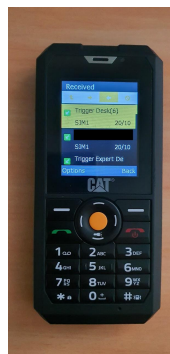
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[6] *LHC Long term Schedule.* URL: https://lhc-commissioning.web.cern.ch/schedule/LHC-long-term.htm

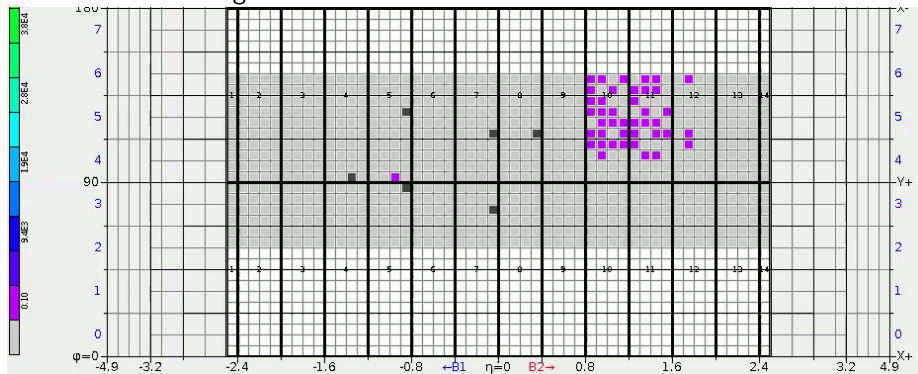# Beam Splashes!

ATLAS Work in Progress

z: Rate (arbitrary units)

- Protons bombard collimator for timing calibrations (lighting up detector)
- A quarter of eFEXs installed at P1 last year with LAr plugged in, monitoring hit rates on very uncalibrated system
- Splashes seen!

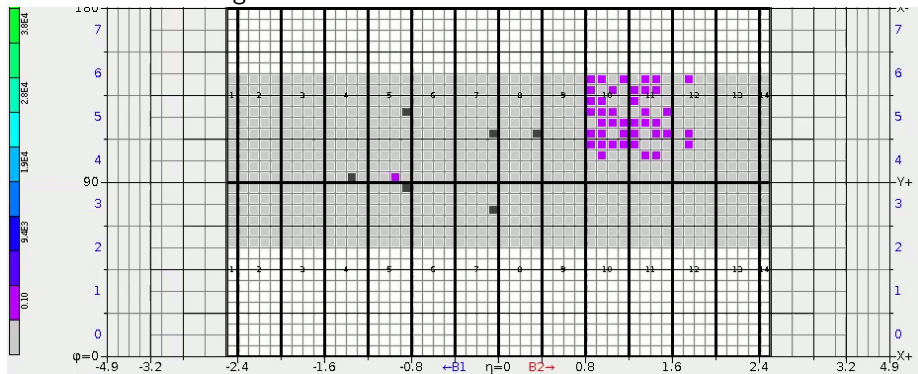# Beam Splashes!

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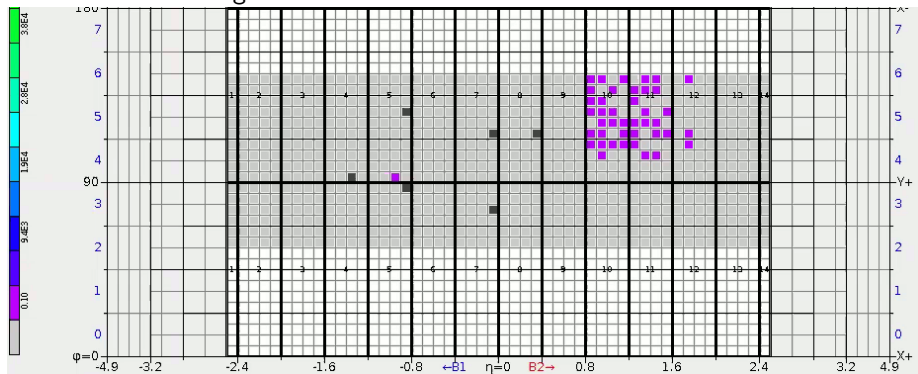# Beam Splashes!

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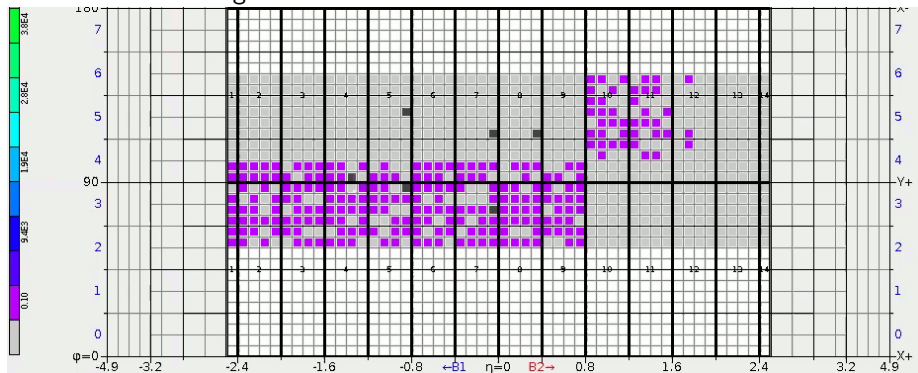# Beam Splashes!

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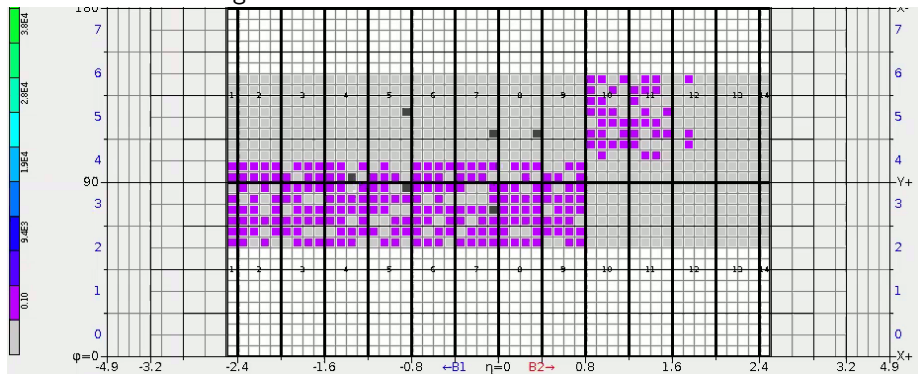# Beam Splashes!

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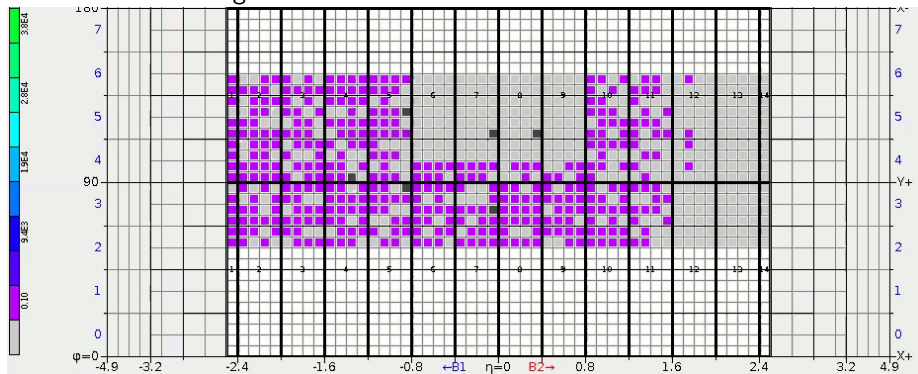# Beam Splashes!

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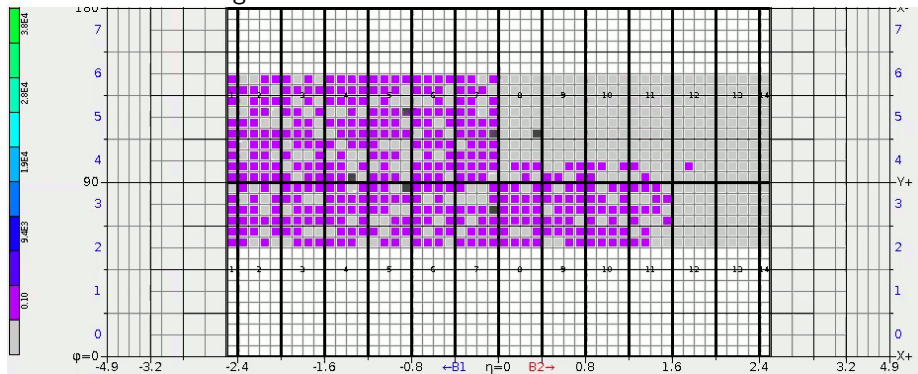# Beam Splashes!

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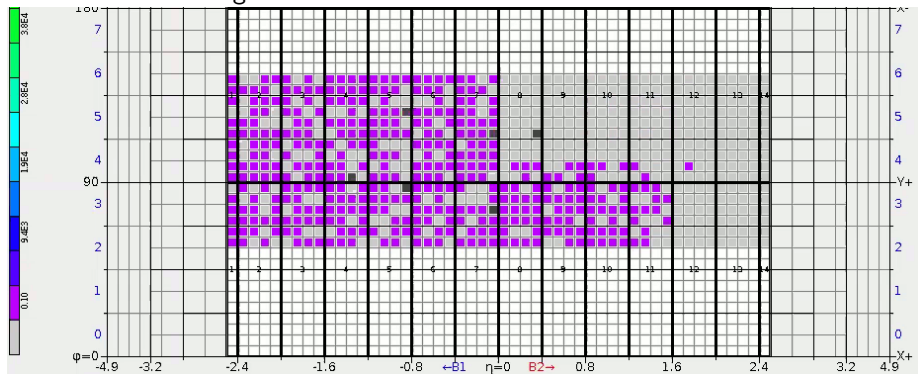# Beam Splashes!

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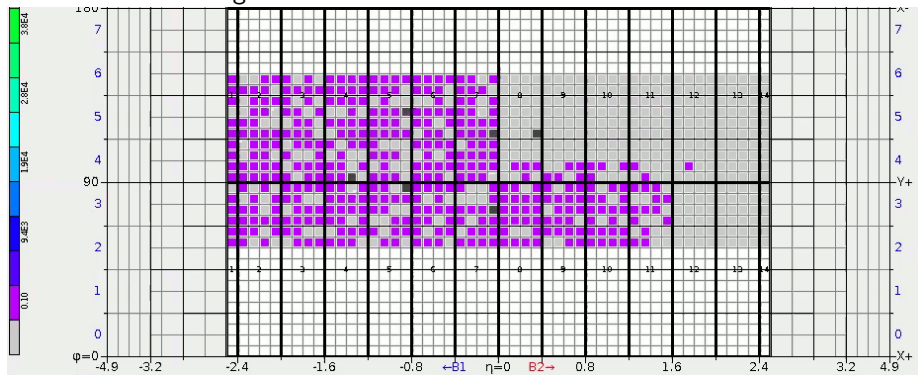# Beam Splashes!

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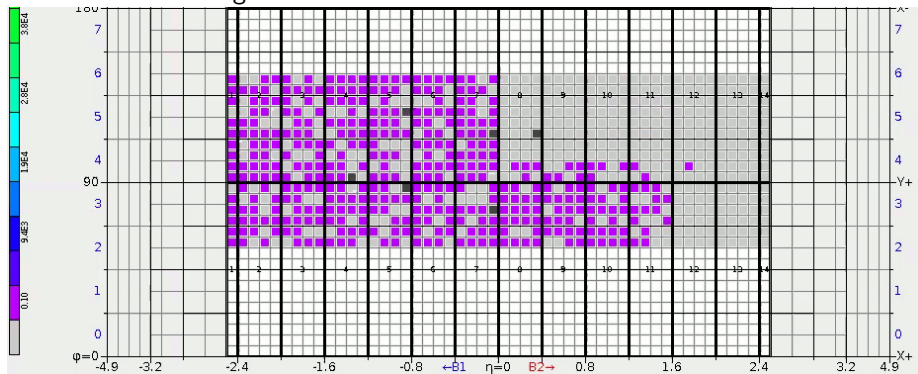# Beam Splashes!

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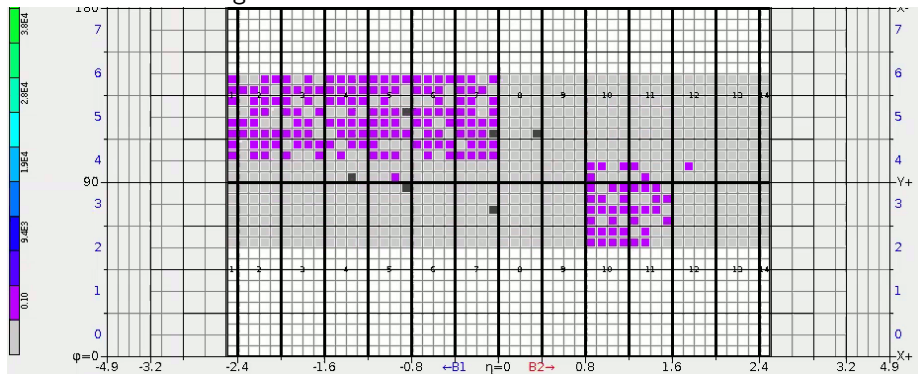# Beam Splashes!

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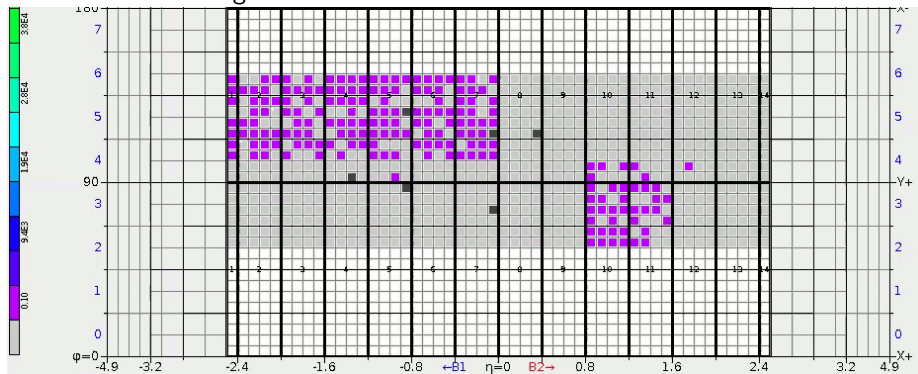# Beam Splashes!

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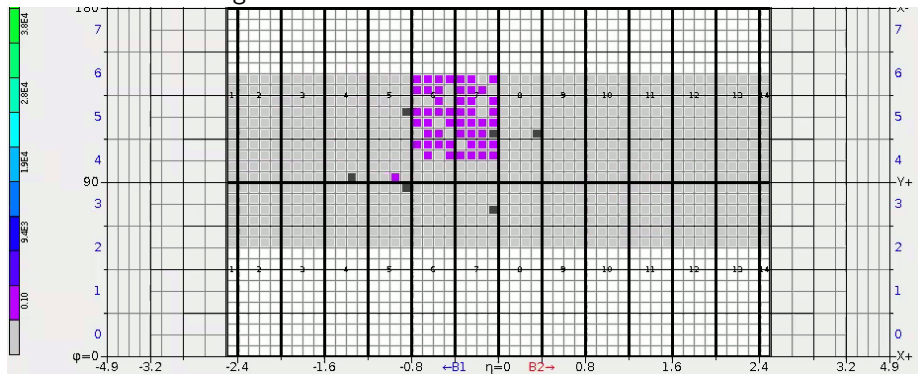# Beam Splashes!

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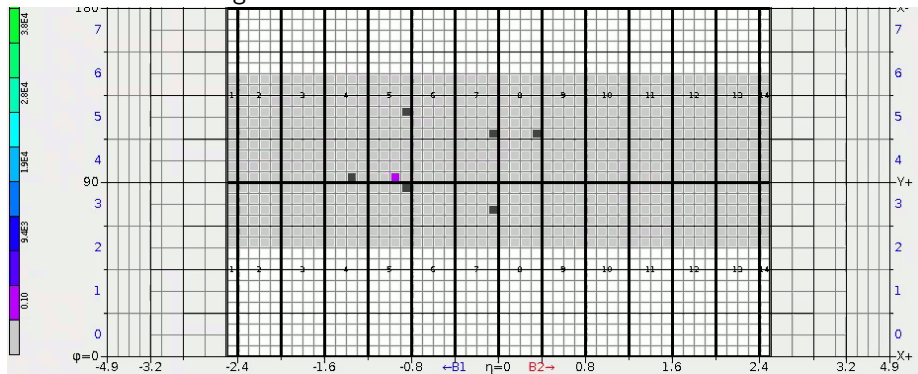# Beam Splashes!

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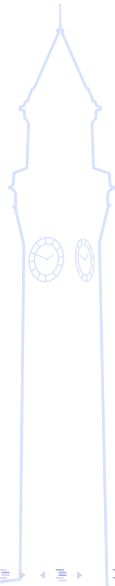- Splashes seen!

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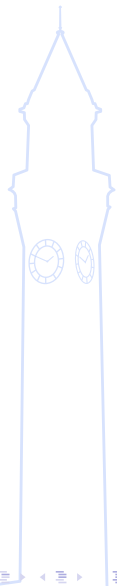ATLAS Work in Progress

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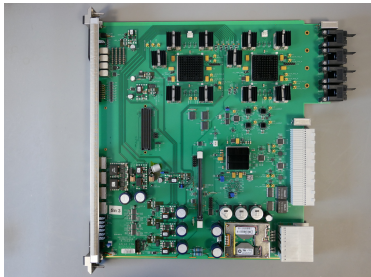- Splashes seen!

Any Questions?

Part V

Backup

The UK Hardware: FTM & ROD

- FEX Test Module (FTM)
- Produces test data patterns that emulate input from other boards and can retrieve outputs for comparison to expectation.
- Invaluable for many tests at CERN and home institutes

- ReadOut Driver (ROD): aggregates read out data within each e/jFEX + Topo shelf for onward transmission to HLT and DAQ