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Image © STFC Alan Ford

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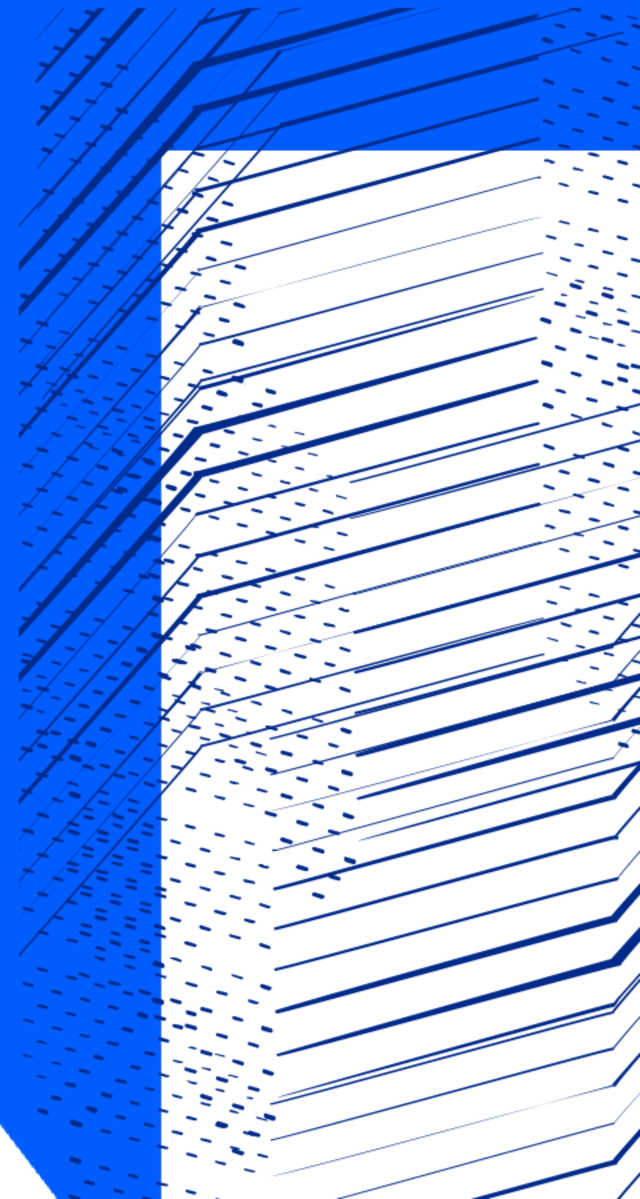
Electronics Integration

Electronics Integration in the UK



Current state of die-level integration

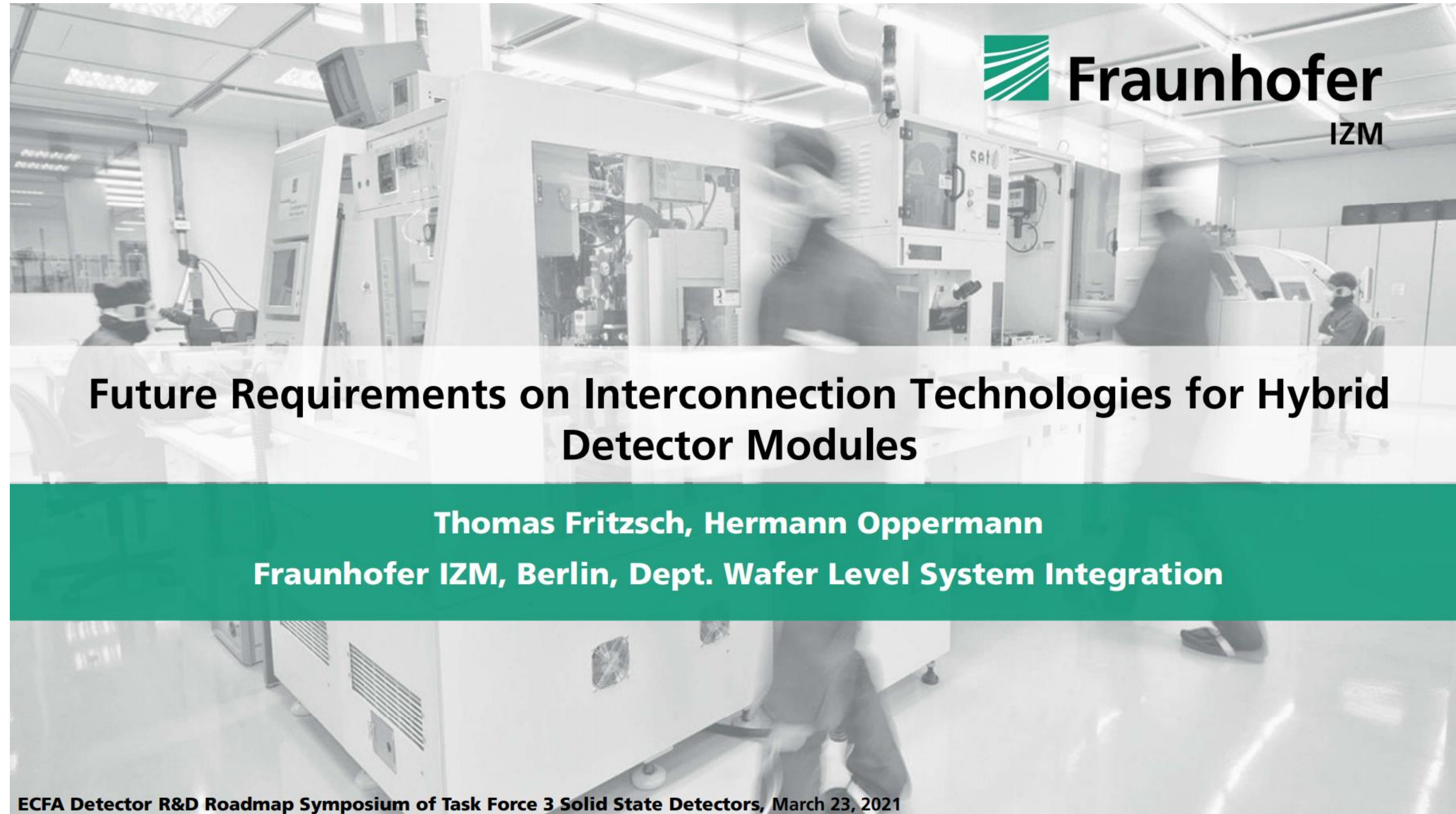
Industry

- Sector locked capabilities (generally not of interest)
  - E.g. Leonardo, BAE systems
- Commercially accessible
  - Micross
  - Alter Technology (incl former Optocap)
  - Ultra
  - CIL
  - III-V Catapult
  - CPI
  - MTC

Academia

- PP/HEP focussed
  - Manchester
  - Liverpool
  - Oxford
  - Cambridge
  - Glasgow
  - Lancaster
  - Edinburgh
  - Sheffield
  - STFC Interconnect
- More general
  - Southampton
  - Loughborough
  - UCL
  - STFC Interconnect

Future requirements overview



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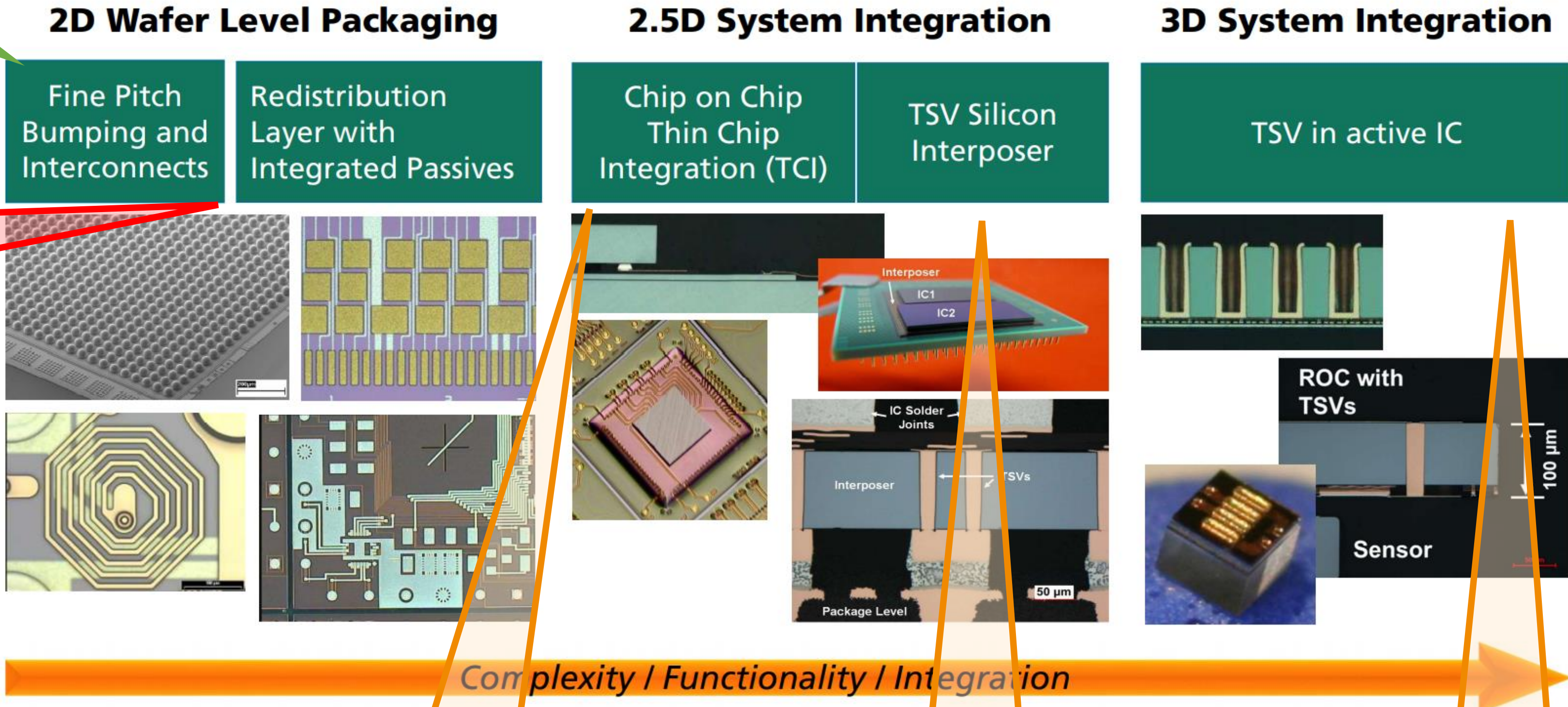
Next few slides map out UK strengths and gaps against T. Fritzsch presentation

ECFA Detector R&D Roadmap Symposium of Task Force 3 Solid State Detectors (23 April 2021) · Indico (cern.ch)

UK has some bumping capability and scattered flip-chip bonding

No known UK activity

Wafer Level Post-Processing Technologies



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Done with bump bonding – need to expand into Cu pillar?

Some experience in other application areas

Some historic developments but no accessible technology

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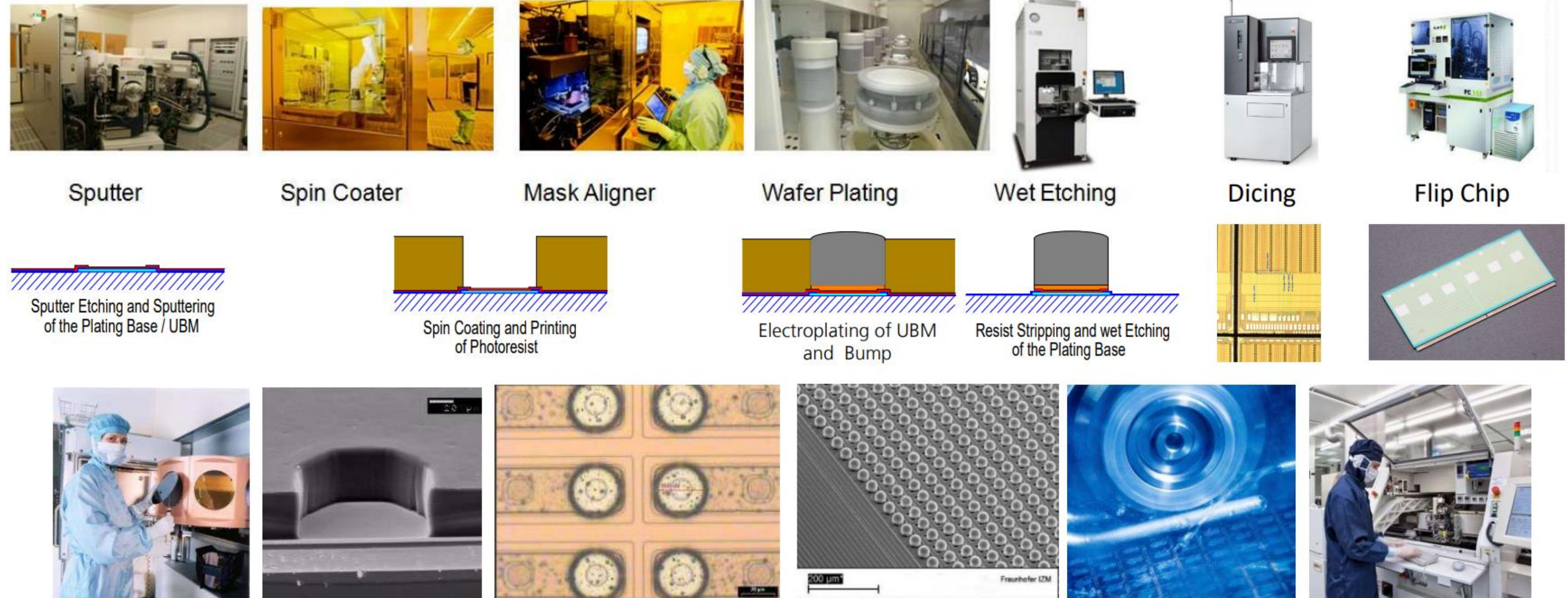
Similar/equivalent processes developed in UK but not (yet) scaled for production

Weaknesses in specific areas to address if required (plate/etch/dice)

Little 300mm capability. Can 200mm be tolerated or what needs scaling?



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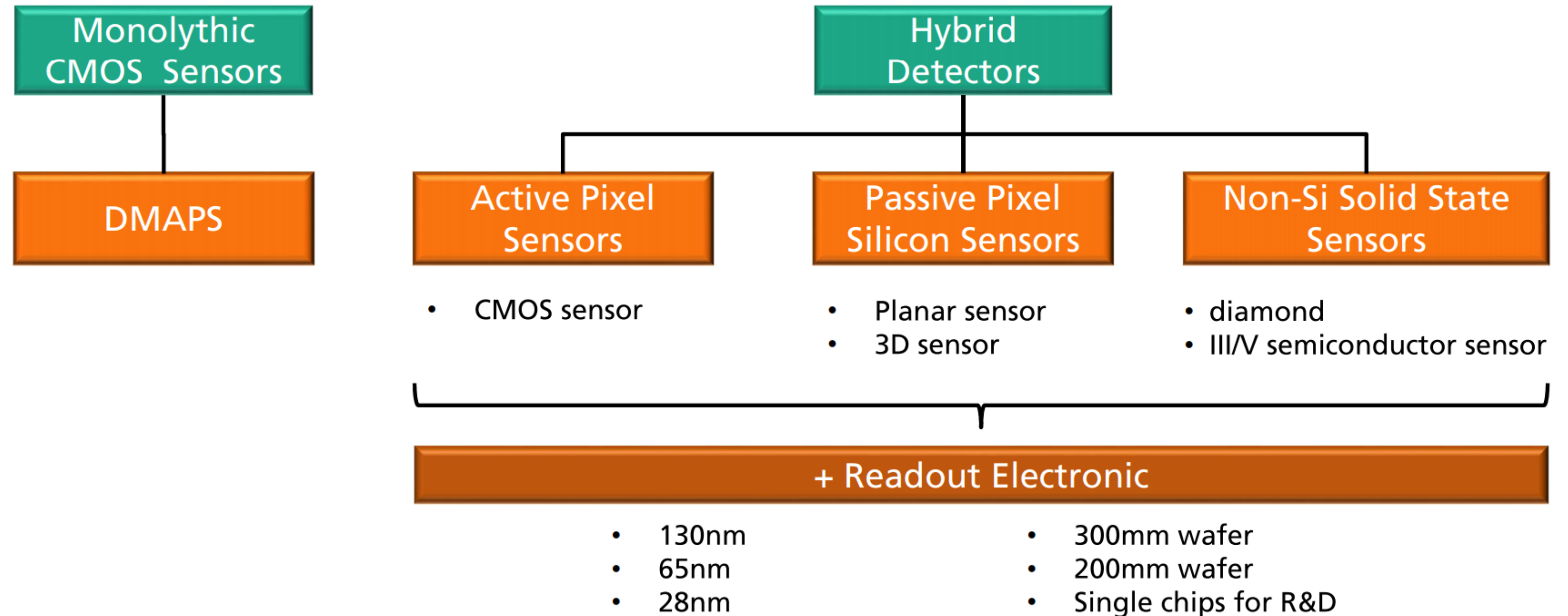
A broad range of technologies requires a broad range of assembly techniques.
Identify areas to build and areas to cut.

- we can't be experts in everything
- Need focussed / targeted investment.



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To address – if important

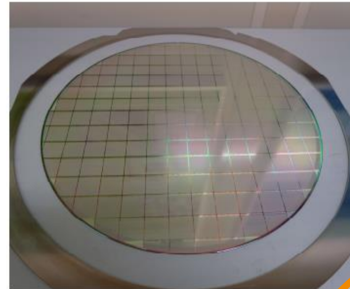
Existing experience – but limited to 200mm

Some relevant experience of 150um on 150mm wafers. No experience at 300mm

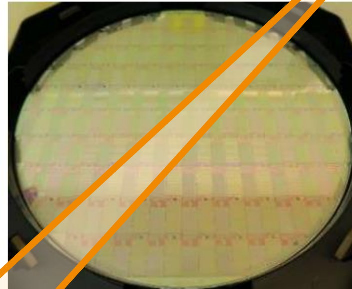
Wafer Substrate Size - Process Line Capabilities

Readout Chip

- 300mm wafer, TSMC 65nm technology
- 132 RD53B/ITKPix readout chips per wafer
- Bumping pitch 50x50 μm²
- RD53B: 400x384 bumps (153.600 chip / 20.275.200 wafer)
- 300mm thin wafer handling (≤ 150μm)



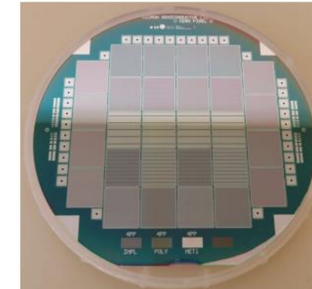
RD53B/ITKPix 300mm ROIC Wafer



RD53A 300mm ROIC Wafer

Sensor Chip

- 150mm sensor wafer: planar or 3D sensor technology
- 200mm CMOS sensor
- UBM deposition process: electro-plating, e-less (NiAu), PVD
- Thin Wafer Handling: 150μm,100μm, 50μm wafer thickness
- Single chip processing with and without carrier



MICRON planar sensor wafer

FBK planar sensor wafer

Wafer Level Post Processing Line for 150mm, 200mm and 300mm Wafer Size required

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PVD established. Other techniques require capital plus development. Some equipment/dev

Some relevant experience of 150um on 150mm wafers. No experience of thinner wafers

Single die method established -> but need to push bump pitch

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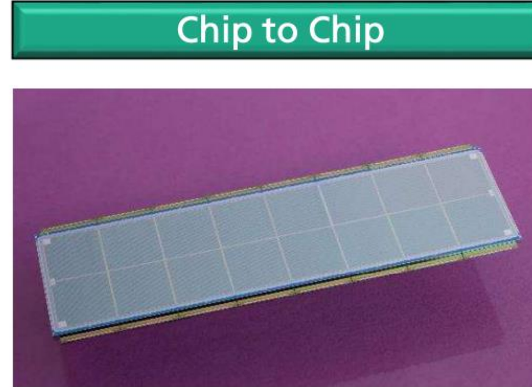
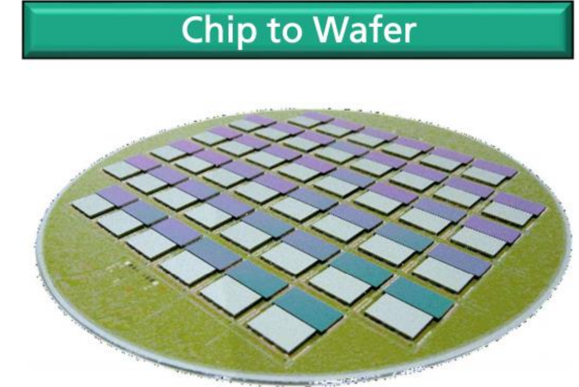
Assembly by Flip Chip Bonding – C2C and C2W

Chip to Chip



Chip to Wafer



Flip Chip Assembly Bonding Tools:

- High accuracy chip pick and place process ≤ 1µm
- Interconnection by temperature and optionally pressure:
    - reflow soldering
    - thermo-compression bonding,
    - thermosonic bonding

Requirements:

- Chuck size: sensor chip size (~10cm) or wafer size up to 300mm and corresponding working space
- Load station (from dicing frame or from waffle pack)
- Consistent with subsequent dicing process
- Advantage: Chips/wafers with different size and pattern can be merged

Equipment and experience

Equipment installed, limited experience

Substantial existing experience. Good equipment installation base

Compatible equipment installed, upgrade options required

Some compatible equipment – upgrades required

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Not aware of any prior knowledge / experience within our communities.

- AML's main line of business
- Clearly key for wafer level, but requires peripheral interconnect exposed via TSV
- More appropriate to wafer fab BEOL than assembly facility (cleanliness)
- Probably contract out if required

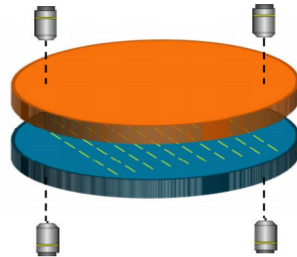
Assembly by Wafer to Wafer Bonding – W2W

Fully/Semi-Automated Wafer Bonder:

- Wafer size 200 mm, 300 mm
- maximum force: 60 kN
- maximum temperature: 550 °C
- vacuum: 1×10^{-5} mbar
- Wafer to wafer alignment accuracy <1µm

Applicable Bonding processes:

- Adhesive bonding
- Silicon direct bonding
- Anodic bonding
- Solder/eutectic bonding
- Thermo-compression bonding
- Metal-oxide hybrid boding



Requirements:

- Wafer size matching: top and bottom wafer of the same size
- Design matching: reticle/chip step and repeat; design/wafer origin
- Particle free and planarized wafer surfaces
- Special processes with pre-assembled wafer possible (parallel KGD assembly)
- Consistent with subsequent dicing process

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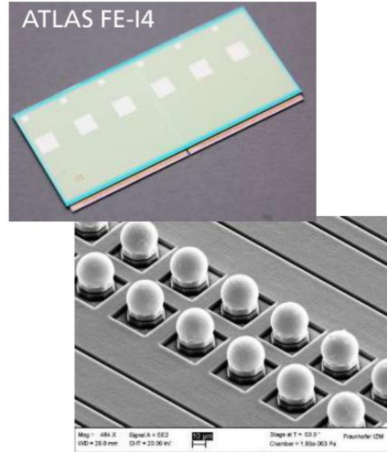
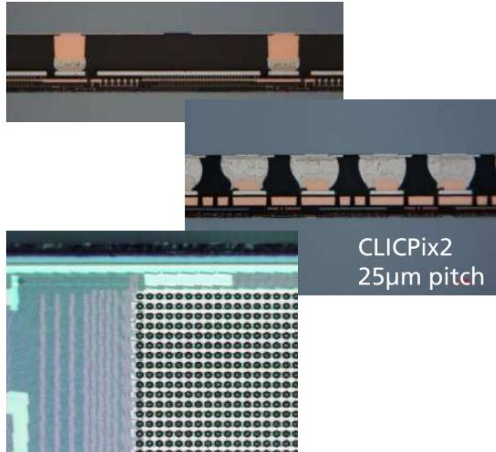
Equipment and experience covers most of listed ranges

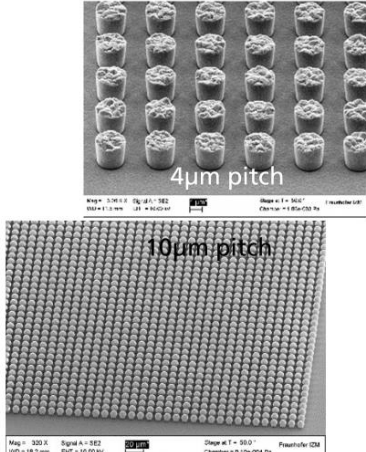
Flip Chip Assembly Key Parameter: Interconnection Pitch



Fine pitch bumping:
Pitch 100…50µm
Bump size: 50…25µm
Material: Solder bumps, pillar bumps with solder cap



µ-bumping:
Pitch 50…20µm
Bump size: 25…12µm
Material: Solder bumps, pillar bumps



Sub-10µ-pitch:
Pitch 10…2 µm
Bump size: 6…1µm
Material: pillar bumps, metal pins

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No prio experience of pillar bumps (only collapse/solder bumps)

We have run bump deposition trials to 2um bump/5um pitch (Indium). Bonding trials have gone as far as 25um pitch. New equipment should allow ~7-10um pitch

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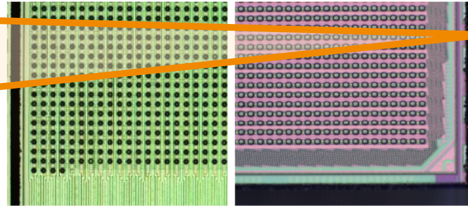
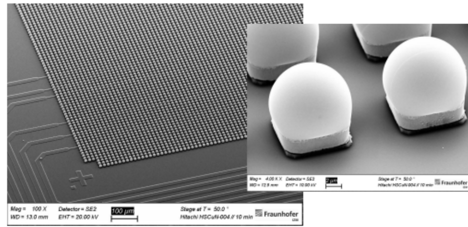
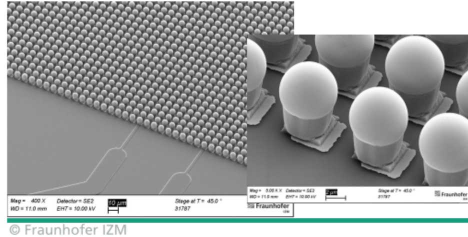
Glasgow/RAL possess some of these and have done some initial processing – no conclusive results yet

Solder Bump Bonding – Bump Size and Bump Pitch Developments

	Bump pitch	Bump size/material	Wafer size
	RD53/ITKPix: 50µm ClickPix2: 25µm	RD53/ITKPix: 50µm SnAg ClickPix2: 17µm SnAg	300mm TSMC65nm Single chips
	IZM Test-chip: 15µm	IZM Test-chip: 9µm In, SnAg	200mm
	IZM Test-chip: 7.5µm	IZM Test-chip: 4µm In, SnAg	200mm

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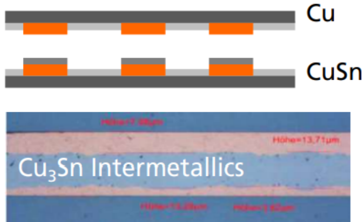
A promising technique, but not in our armoury – probably most appropriate in W2W BEOL facilities

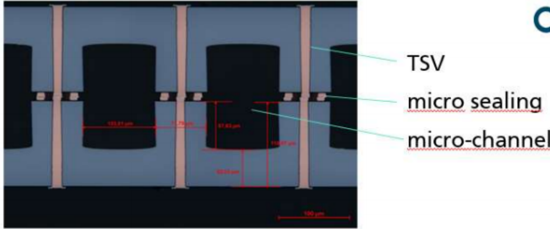
Transient Liquid Phase Bonding (TLPB) / Solid Liquid Interface Diffusion (SLID)



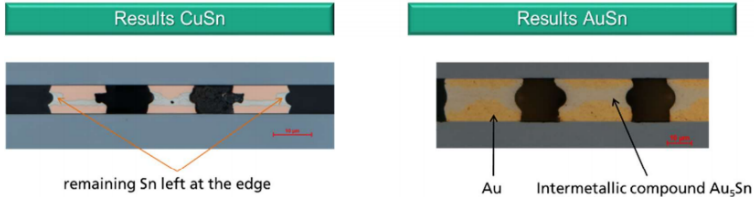
- ECD Cu and Cu-Sn pads
- High melting Cu_3Sn IMC (676°C)
- Bonding parameters: 220…280°C, 10…50MPa, T= min
- High planarity necessary
- Inert atmosphere required

Hermetic Sealing

Silicon interposer:
2 half-shells forming a microchannel cooler



4-port fludic interposer



Process available for C2C, C2W, W2W assembly

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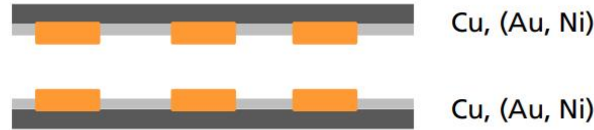
No UK focus

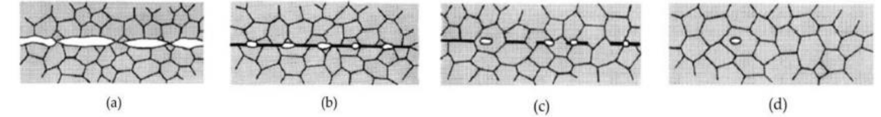
Probably best technique for bonding CTE matched materials. Not good for mismatched (limited application)

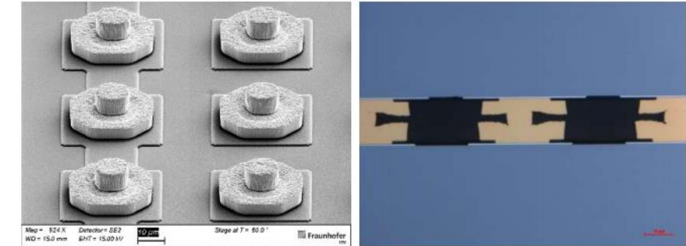
Some relevant experience on single die, Au-Au bonding

Bonding without Solder: Metal-Metal Diffusion Bonding



- ECD Cu pads (Au, Ni)
- Planarized surfaces, pre-conditioning
- Bonding parameters:
  - 250°C…400°C,
  - 50…150MPa
  - t= min…h
  - Noble metal contacts or bonding in inert atmosphere
- Interconnection for 3D chip stacking





Au-μ-pillar after metal-metal bonding onto Au pad

Reduction of Bonding Force – MEDIPIX3 size chip 256x256 pads:

- Regular pad size: 30μm, 150MPa → ~7kN bonding force per chip
- Pillar pad: 10μm, 150Mpa → 770N bonding force per chip

Process available for C2C, C2W, W2W assembly

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C2C & C2W possible on already installed UK flip chip equipment

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Holy grail for enabling minimal dead area tiled areas.
High value, high complexity means significant barrier -> not economically suited to low volumes or occasional fabrication

No UK focus

TSV Integration Schemes

Via first or middle

BEOL
front end
TSV
Si-bulk

- TSV integration before FEOL or after FEOL / before BEOL
- Processes established at IDMs

Front Side - Via last

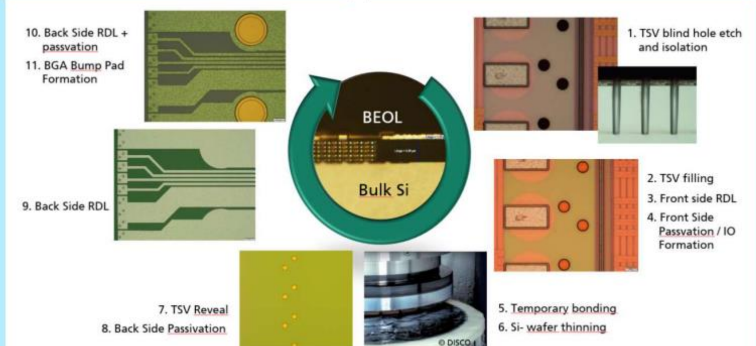
BEOL
front end
TSV
Si-bulk

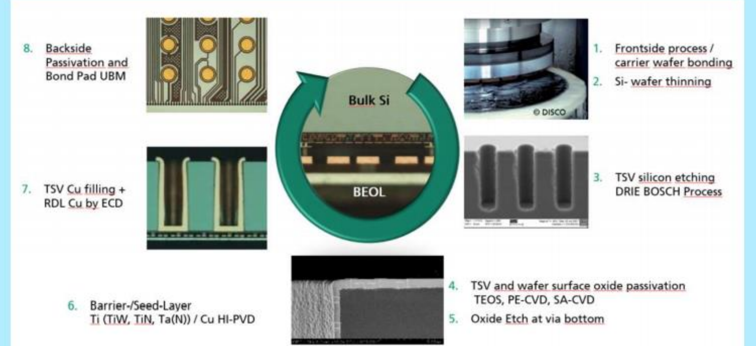
- TSV integration after complete wafer processing, etch TSV through thick BEOL oxide
- Requires keep out zones in FEOL and BEOL for TSV integration

Back Side - Via last

Si-bulk
TSV
front end
BEOL

- TSV integration after complete wafer processing
- Requires TSV adapted landing pad design in BEOL for TSV connection





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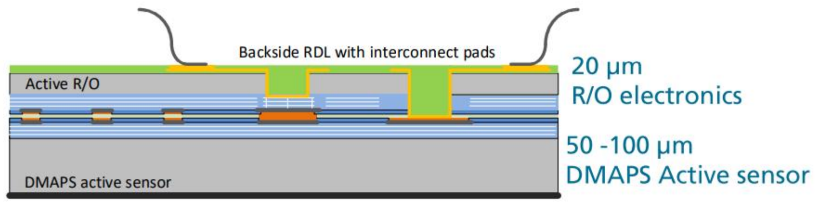
Of particular/niche value to low mass projects such as particle trackers and BSI devices.

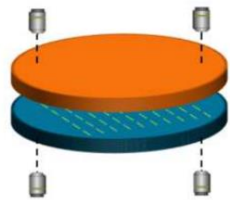
Ultra Thin Hybrid Pixel Detectors

- R/O backside redistribution layer (RDL) with contact pads
- Thinned R/O wafer with backside via last interconnection
- Bonding layer with metal-metal or capacitively coupled contacts
- Thin DMAPS sensor with contact pads and backside processing



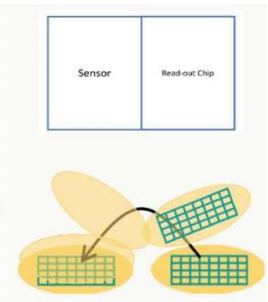
20 µm
R/O electronics

50 -100 µm
DMAPS Active sensor



Develop dedicated CMOS Sensor wafer compatible with a pixel FE chip wafer:

- Starting point: passive CMOS sensor development on 200 mm wafer with 110/150 nm process node from LFoundry
- Use either TimePix3 chip wafers (130 nm on 200 mm wafers) or own FE development on the same wafer as the sensor
- Develop and optimize hybridization process including thinning and interconnection from chip's backside
- Transfer process to more modern feature size pixel chips (65nm or 28 nm on 300 mm wafers) for smaller pixel pitches and faster electronics (long term, not with AIDAinnova)



Modest experience of manual handling thinned wafers and die.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

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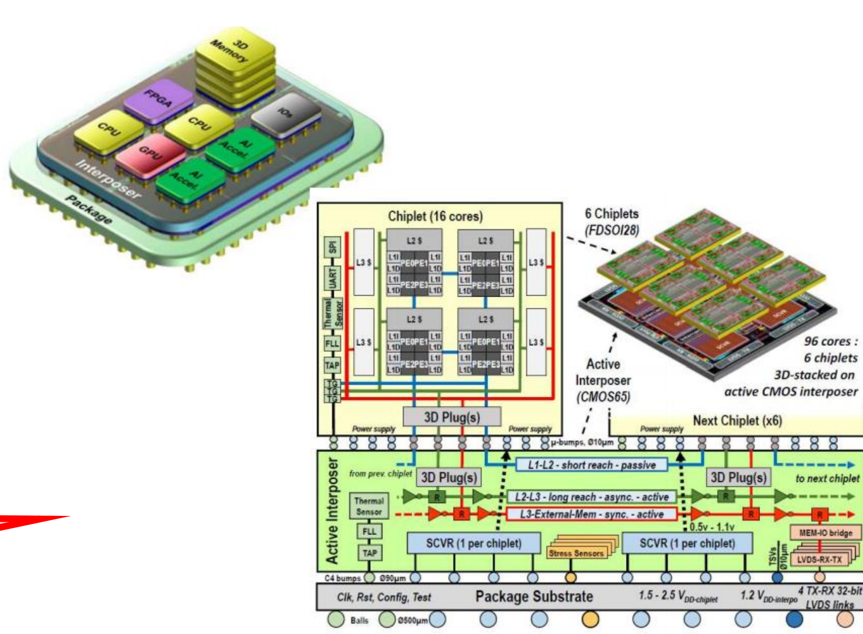
Attractive means of increasing yield. Shifts emphasis from chip to interconnect yield. Increased die count.

No current UK focus

Industry Technology Trend: Processor Chiplet Assembly on Active Interposer



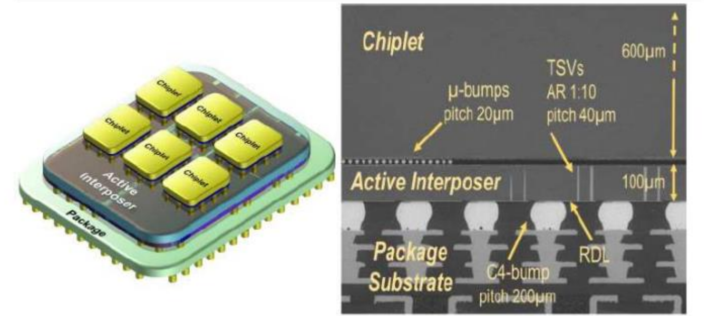


Fig. 5. INTACT : from concept to 3D-cross section

TABLE I: INTACT MAIN CIRCUIT FEATURES AND 3D TECHNOLOGY DETAILS

Chiplet technology	FDSOI 28nm, 10 metals, 0.5V-1.3V+adaptive biasing
Chiplet area	4.0 mm x 5.6 mm = 22.4 mm²
Chiplet complexity	395 Million transistors, 18 transistors/µm² density
Interposer tech.	CMOS 65nm bulk, 7 metals, MIM option, 1.2V
Interposer area	13.05 mm x 15.16 mm = 197.8 mm²
Interposer complexity	15 Million transistors, 0.08 transistors/µm² density
3D technology	Face2Face, Die2Die assembly onto active interposer
µ-bump technology	Ø10µm, pitch 20µm
#µ-bumps	150 000 (20k signals + 120k powers + 10k dummies)
Inter-chiplet distance	800µm
TSV technology	TSV middle, Ø10µm, height 100µm, pitch 40µm
#TSV	14 000 TSV (2 000 signals + 12 000 power supply)
Backside RDL	10µm width, 20µm pitch
C4-bumps	Ø90µm, pitch 200µm, 4,600 bumps
Flipchip package	BGA 39 x 39, 40mm x 40mm, 10 layers
Balls	Ø500µm, pitch 1mm, 1 517 balls

Pascal Vivet, Eric Guthmuller, Yvain Thonnart, Gaël Pillonnet, Cesar Fuguet, et al.. IntAct: A 96-Core Processor With Six Chiplets 3D-Stacked on an Active Interposer With Distributed Interconnects and Integrated Power Management. IEEE Journal of Solid-State Circuits, Institute of Electrical and Electronics Engineers, 2020, pp.1-1. 10.1109/JSSC.2020.3036341 . hal-03072959

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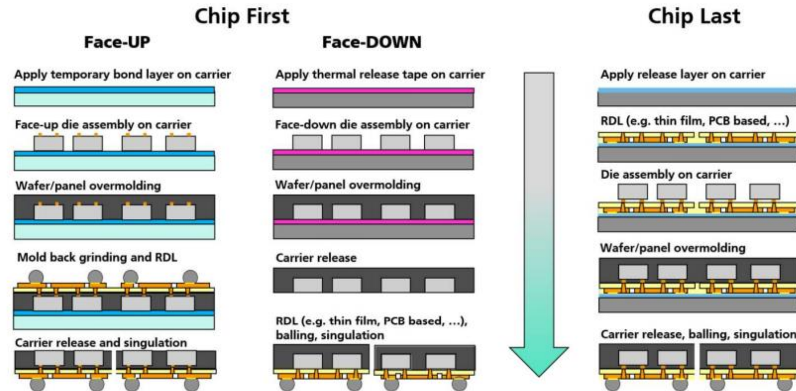
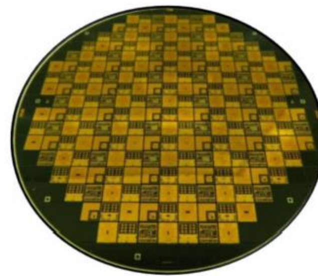
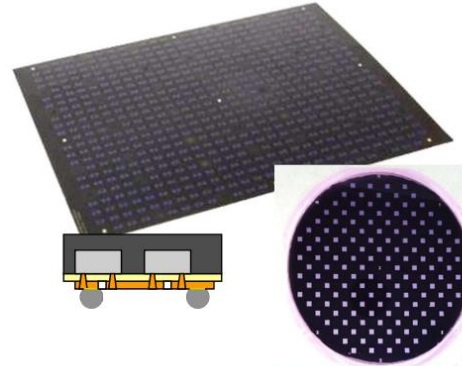
Standard BEOL processes.
Doubtful that we'd build facilities to do this.
Instead: out-source to wafer fabs, build useful relationships

Industry Technology Trend: Embedding and Fan-Out Wafer Level Packaging





IZM MPW mold-compound wafer



- KGDs embedded in a mold-compound on 200mm, 300mm wafer level or panel level
- Thin film post processing at wafer or panel level
- Chip IOs connected via thin film fan-out RDL, in most cases for SiP assembly onto PCB
- Thinning and dicing using regular post processing equipment and processes

Possible benefits for HEP:

- Can be used for serial powering?
- pre-assembled stave-structures?
- Others?

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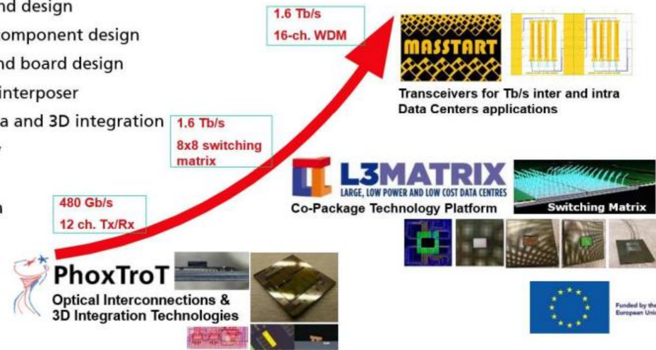
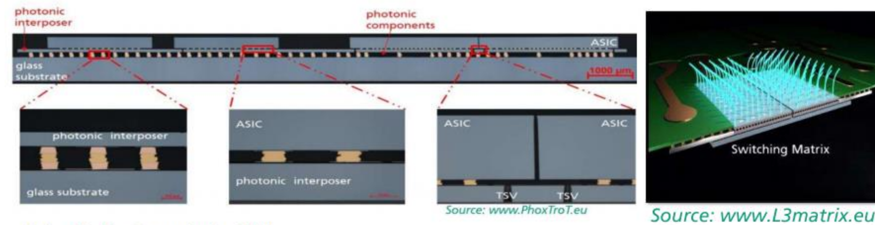
Probably use in commercial blocks, rather than build ourselves.
If fabrication is needed, engage with photonics cluster around Torquay?

Industry Technology Trend: Photonic Integration Technology

Empowering Photonic Interconnects for Data Center and NGC

- System concept and design
- Photonic and RF component design
- Signal integrity and board design
- Silicon photonics interposer
- Through silicon via and 3D integration
- Flip chip assembly
- Co-package
- System evaluation
- Benchmarking





Switching Matrix

Source: www.L3matrix.eu

Tolga Tekin, Fraunhofer IZM

New technological paths for high performance chips targeting HPC and edge, EXDCI Workshop, Brussels, 05. - 06.11.2019

- High data rate communication using Photonic IC (PIC)
- Drivers in Industry: next generation computing - cloud, edge, node HPC
- Electrial and optical integration on silicon photonic interposer and PIC
- Optical off-chip interconnection for chip-to-chip communication: low-latency, high-bandwidth, high density, low power
- Massive switching beyond 400 Gb/s with new developed Serializer/Deserializer cicuits and optical links

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300mm necessitates fewer fab facilities -> greater reliance on constructive relationships

Look at defragmenting the scattered capabilities

Increasing demand – key to future

Conclusions

- 65nm and 28nm readout electronic chips will be produced on 300mm wafer:
  → requires 300mm post process line for R&D and production - 2D only or fully equiped 3D line?
  → MPW single chips: post processing for R&D
- Sensor wafer 100mm? – 150mm – 200mm wafer size:
  → additional post processsing line for these wafer sizes
  → diamond sensor: single chip post processing?
- Ultra thin wafer handling:
  → 100µm…50µm..20µm with temporary/permanent carrier concepts
  → 150mm, 200mm, 300mm wafer size
- Concepts for C2W and W2W hybridization:
  → start this already at design level
  → keep it simple, more reticle stepper pattern than „pizza" design
- Different bonding processes are available for C2C, C2W and W2W:
  → some restrictions in availability due to patent protection
- Adaption of trends from industry for integration technologies, i.e.
  → chiplet stacking
  → embedding and fan-out packaging
  → photonic packaging

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Do project needs exist?

Evaluate usefulness

No current UK academic focus – enter with care (licensing).

It is clear that

- Future interconnect capability to be driven by science and detector requirements
- UK has some significant existing specialisms due to prior investments (mainly around hybrid pixel detector assembly) – should we be building on these or shifting to new?
- We have some initial experience in areas such as thin die/wafer handling & metal-metal bonding
- UK has no capabilities in some other (potentially key) areas – do we secure access through collaboration or establish by some other means?
  - Need access strategy (per process):
    - Buy from UK industry
    - Buy from industry elsewhere
    - Build a capability
    - Team up so that a capability is established across multi-sites/ multi-orgs
- As many processes are higher value, trend will be towards minimal number of implementers, with others needing access mechanisms. No-one is big enough to do everything – so coordinated approach required.

- Key areas to consider:
  - Handling of thinned wafers/die – a recurring and increasingly frequent theme, but not for all!
  - C2W and W2W – select processes which will map to future projects

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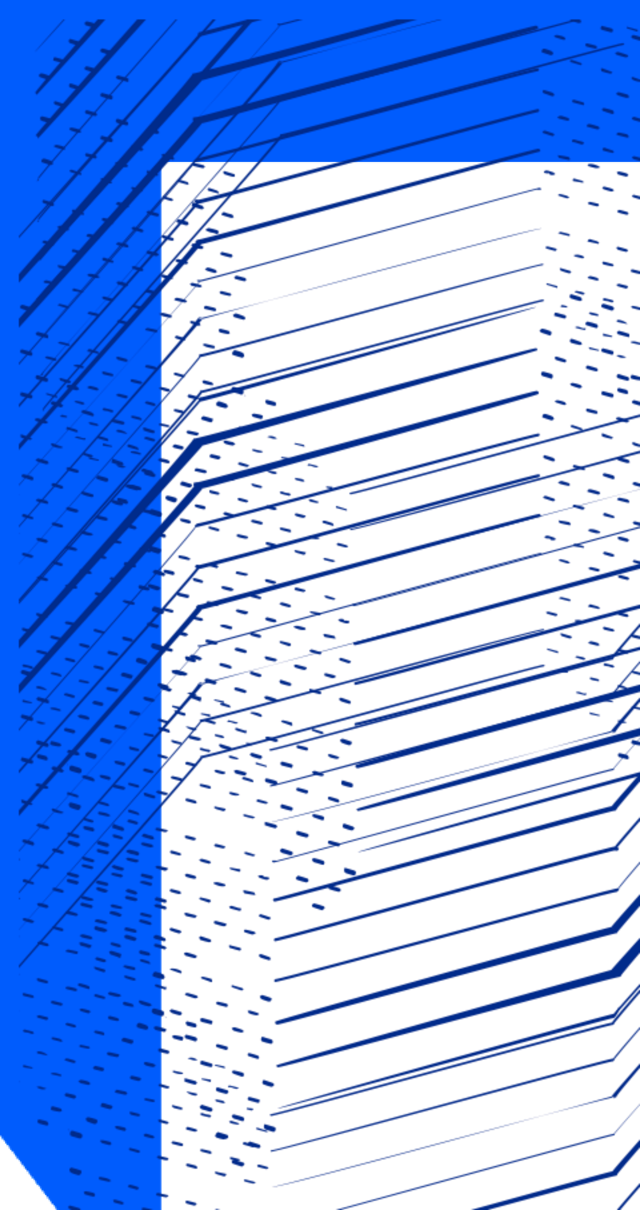
STFC Interconnect

Equipment and experience relevant to future Electronics Integration

(Backup slides)



STFC Interconnect detector assembly facility

Opened Nov 2019

A home for:

ATLAS detector upgrade assembly - opening the door to new discoveries
Flip chip assembly process - producing STFC's detectors
ASIC integration - supporting design to delivery
CMOS sensors - system integration and test

Wire bonding

Al-wedge machines:
2 x Hesse BJ 820
1 x Hesse Bondjet 715

Au-ball machine:
Palomar 8000

Hybrid machines (ball & wedge)
1 x Hesse BJ 855
1 x F&K Delvotek manual bonder

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Glue dispense

3 options:
Glue dispense
Glue dispense auger screw delivery
Stencil printing

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Die attach

Dr Tresky die placer
FC150 Flip chip machine
FC300 Flip chip machine

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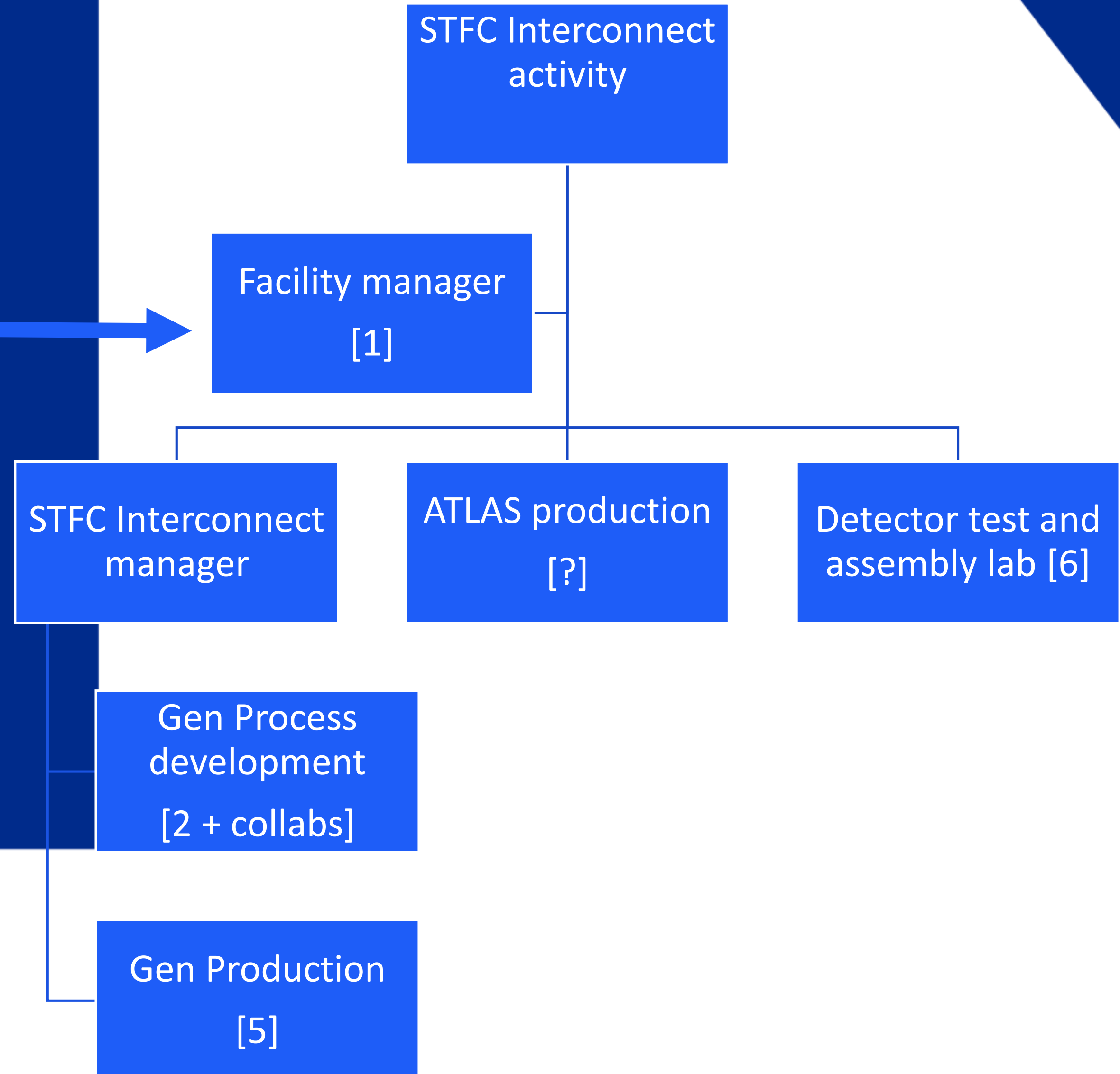
Team structure

Current structure

Future structure ???



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