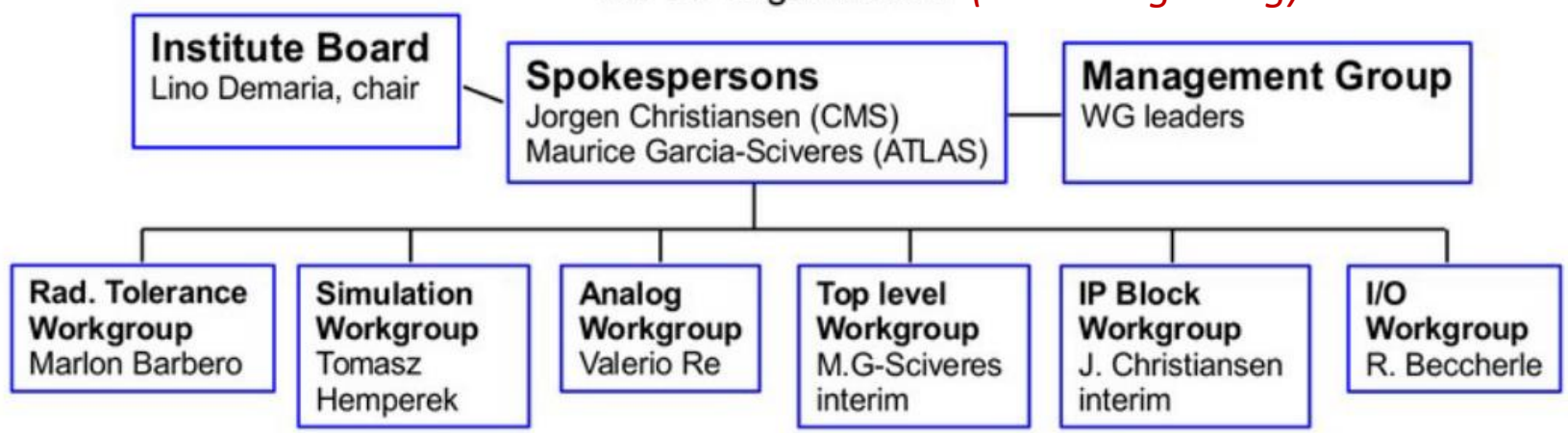
Science and Technology Facilities Council

RAL ASIC Design Group
Recent R&D experience

Mark Prydderch – ASIC Design Group Leader

mark.prydderch@stfc.ac.uk

RD53 Collaboration



Collaboration meeting RAL 2014

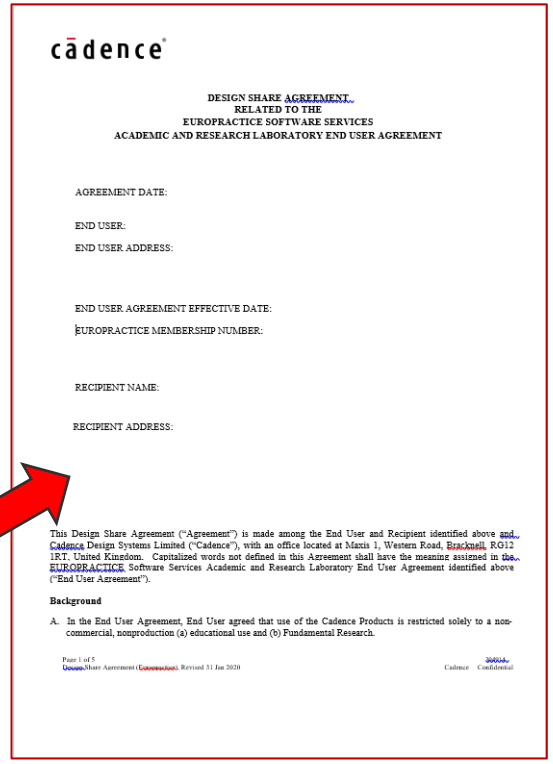
- Clear challenges & goals for collaboration
- Collaboration structure – Clear decision making processes
- Collaboration membership rules
- Collaboration agreement/MoU – including IP sharing
- Funding – Needs to be secure for duration of participation

We were reliant on internal funding

- Meetings & workshops, Email groups, Web site…
- Documentation – Publications, author list, approvals
- Secure shared database for designs (CLIOSOFT)

Cadence Design Share Agreement might now be a barrier to doing this, or at least a hindrance

The extent to which CERN's proposed 28nm NDA is available to institutes might also be an issue in future…



cadence

DESIGN SHARE AGREEMENT
RELATED TO THE
EUROPRACTICE SOFTWARE SERVICES
ACADEMIC AND RESEARCH LABORATORY END USER AGREEMENT

AGREEMENT DATE:

END USER:

END USER ADDRESS:

END USER AGREEMENT EFFECTIVE DATE:

EUROPRACTICE MEMBERSHIP NUMBER:

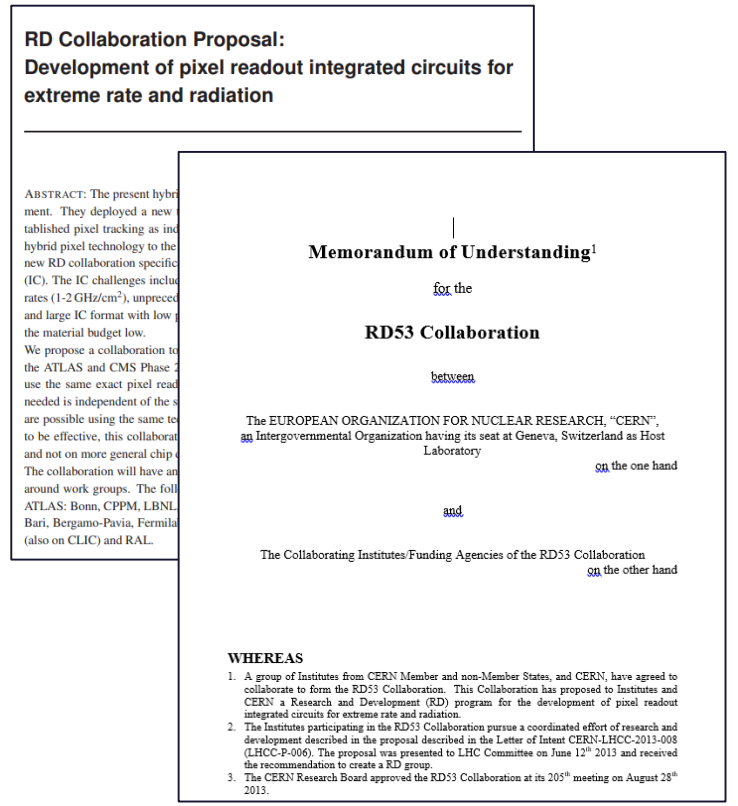
RECIPIENT NAME:

RECIPIENT ADDRESS:

This Design Share Agreement ("Agreement") is made among the End User and Recipient identified above and Cadence Design Systems Limited ("Cadence"), with an office located at Maxis 1, Western Road, Bracknell, RG12 1RT, United Kingdom. Capitalized words not defined in this Agreement shall have the meaning assigned in the EUROPRACTICE Software Services Academic and Research Laboratory End User Agreement identified above ("End User Agreement").

Background

A. In the End User Agreement, End User agreed that use of the Cadence Products is restricted solely to a non-commercial, nonproduction (a) educational use and (b) Fundamental Research.



RD Collaboration Proposal:
Development of pixel readout integrated circuits for extreme rate and radiation

ABSTRACT: The present hybr
ment. They deployed a new
tablished pixel tracking as ind
hybrid pixel technology to the
new RD collaboration specific
(IC). The IC challenges inclu
rates (1-2 GHz/cm^2), unprece
and large IC format with low
the material budget low.
We propose a collaboration to
the ATLAS and CMS Phase
use the same exact pixel read
needed is independent of the
are possible using the same te
to be effective, this collaborat
and not on more general chip
The collaboration will have an
around work groups. The foll
ATLAS: Bonn, CPPM, LBNL,
Bari, Bergamo-Pavia, Fermila
(also on CLIC) and RAL.

Memorandum of Understanding[1]

for the

RD53 Collaboration

between

The EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH, "CERN", an Intergovernmental Organization having its seat at Geneva, Switzerland as Host Laboratory
on the one hand

and

The Collaborating Institutes/Funding Agencies of the RD53 Collaboration
on the other hand

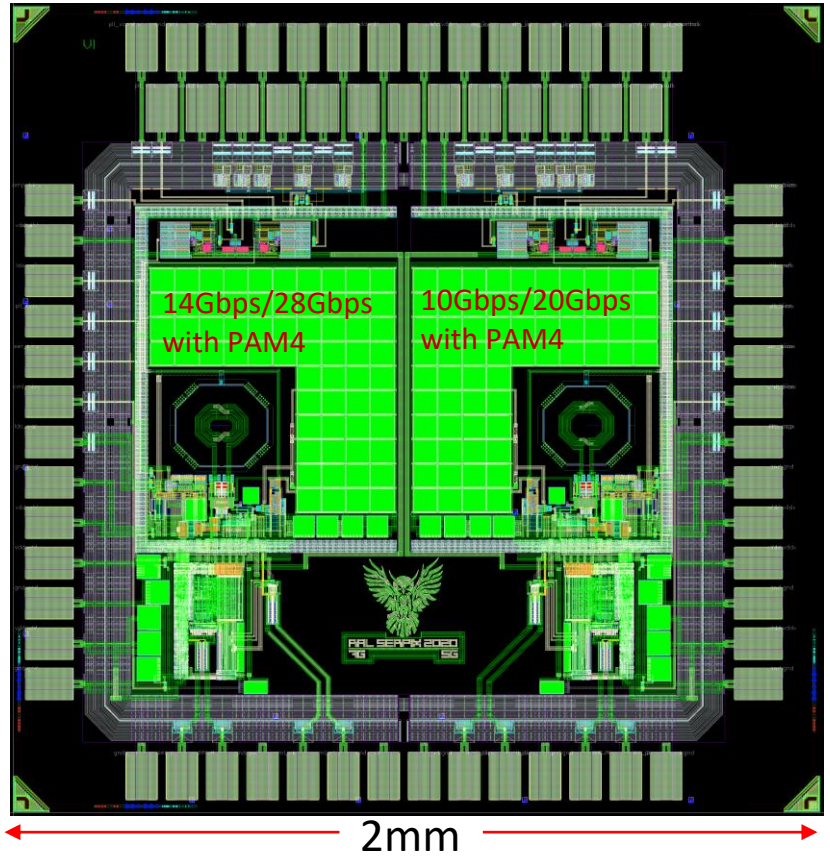
WHEREAS

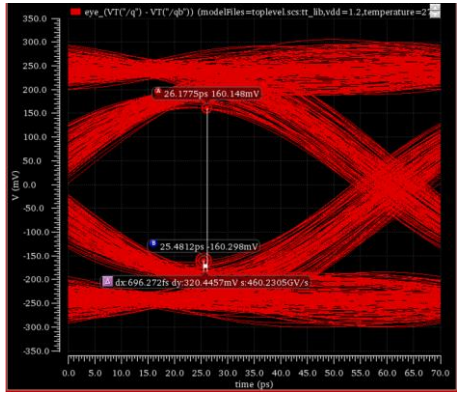
1. A group of Institutes from CERN Member and non-Member States, and CERN, have agreed to collaborate to form the RD53 Collaboration. This Collaboration has proposed to Institutes and CERN a Research and Development (RD) program for the development of pixel readout integrated circuits for extreme rate and radiation.
2. The Institutes participating in the RD53 Collaboration pursue a coordinated effort of research and development described in the proposal described in the Letter of Intent CERN-LHCC-2013-008 (LHCC-P-006). The proposal was presented to LHC Committee on June 12th 2013 and received the recommendation to create a RD group.
3. The CERN Research Board approved the RD53 Collaboration at its 205th meeting on August 28th 2013.

Internal IP development programme

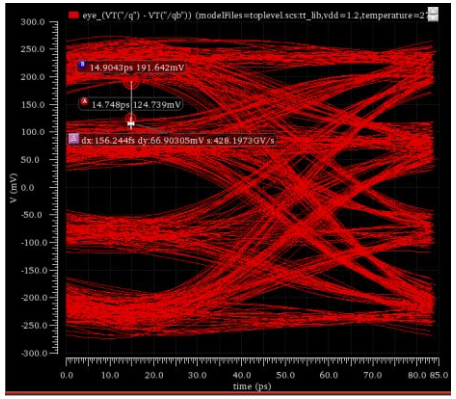
- Limited funding subject to approval & yearly finances
- Developing experience with new technologies
- IP not exclusive to Particle Physics applications
- Starting to explore 28nm with further IP development planned

65nm Serializers with PAM4 option

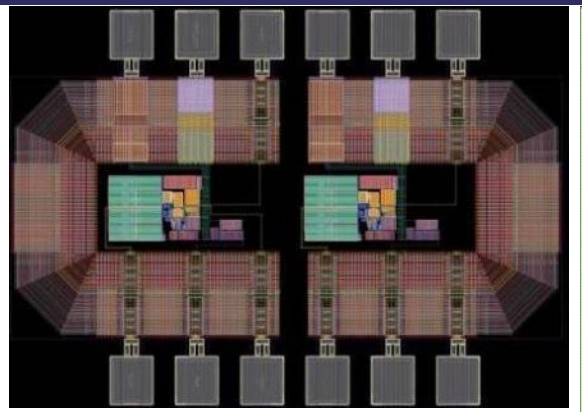




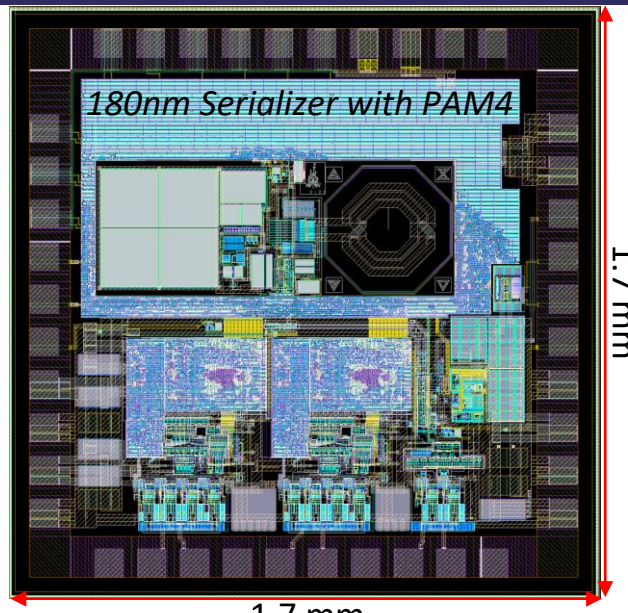
NRZ simulation

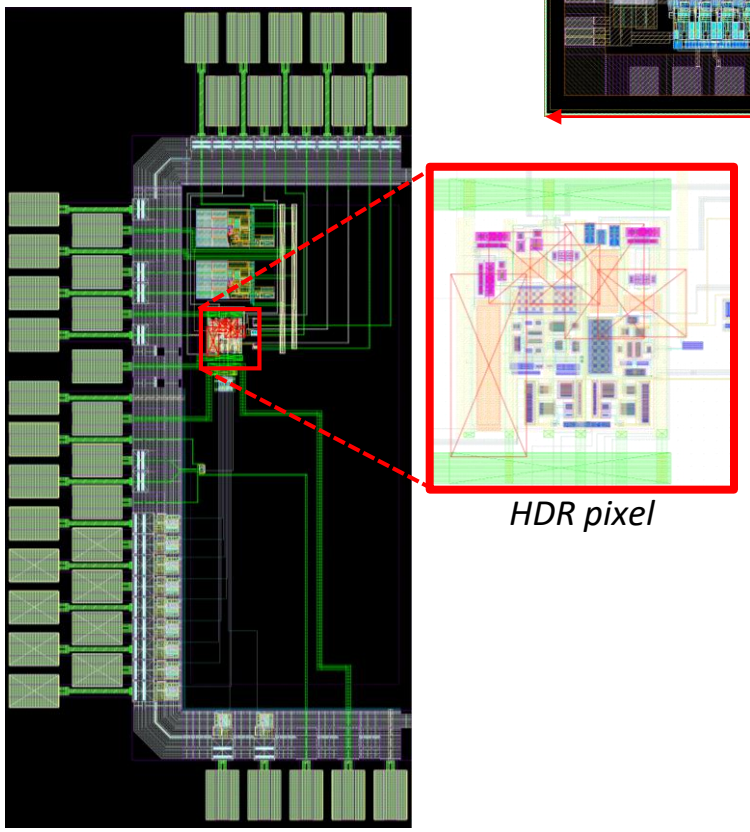


PAM4 simulation



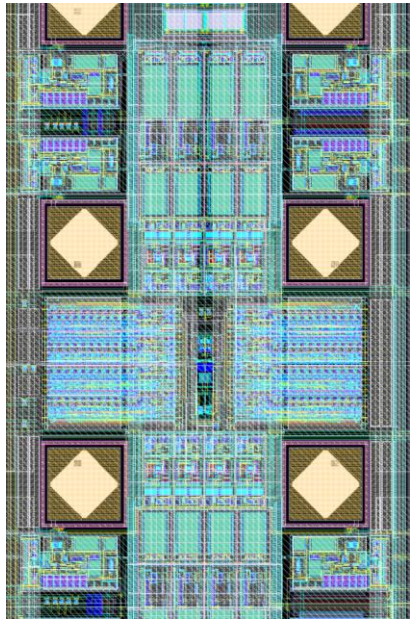
Rail-to-rail Voltage Driver for RD53





Direct-to-Digital Test Structure

HDR pixel



1.6GHz Dual-clock-edge 12-bit TDC

Science and Technology Facilities Council

Thank you

Facebook: Science and Technology Facilities Council

Twitter:@STFC_matters

YouTube: Science and Technology Facilities Council