Implementation of a new mode into the interlock system on normal-conducting magnet failure

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Motivation for this R&D

- Any failures of beamline magnets can cause a serious damage on the beamline equipment. Toward the 1.3MW, enhancement of the interlock system is important.
- We have implemented an interlock system on the normal-conducting magnet failure so far but it's effective only for current drop (e.g. failure of the power supply of the magnets).
- In this R&D, we will add a new mode into the interlock system. This can detect any voltage drop which can be occurred in case the magnet failure (e.g. inter-coil short)
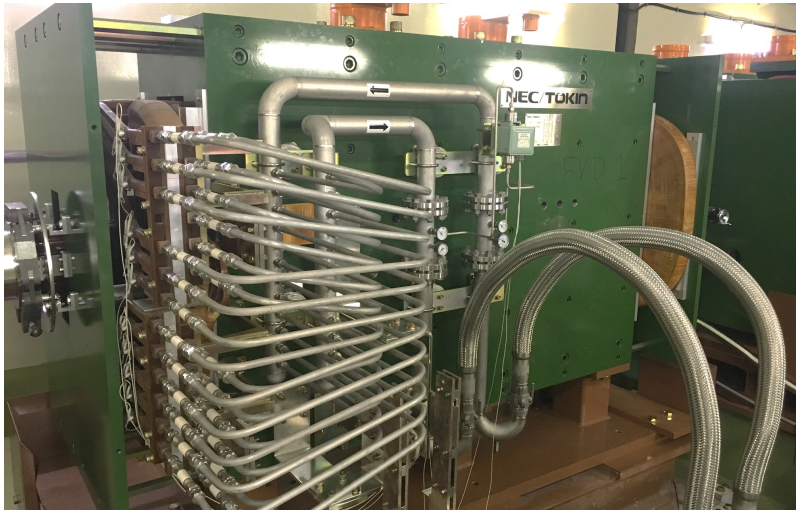

Magnets at primary beamline

Required interlock latency

- If the magnetic field fluctuates by 5%, the beam hits the equipment and destroys it, so implement an interlock that detects 1% fluctuations.
- The interlock alarm time of the current fluctuation interlock was 6 msec. New interlock should have lower latency than existing one.

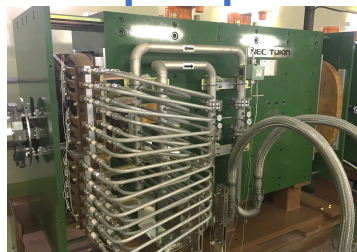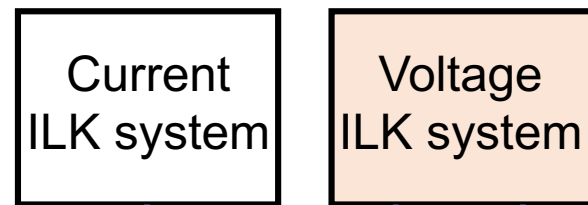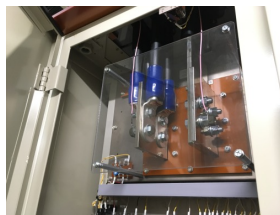**To prevent any damage of beamline equipment**

One of bending magnets at primary beamline
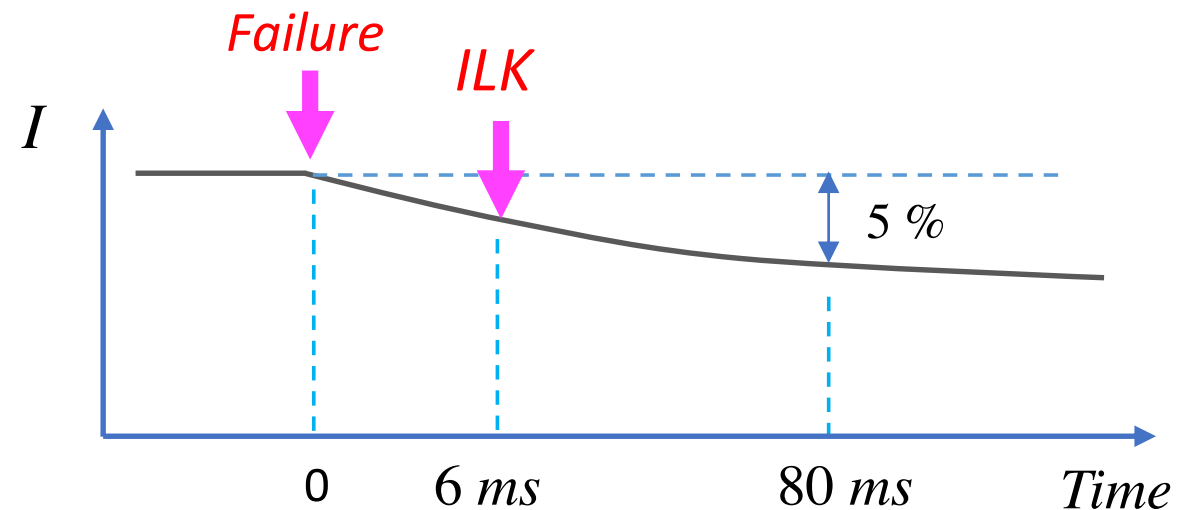
Current decay curve of a real magnet (measured)

A new mode into the interlock system on normal-conducting (NC) magnet

Power supply

New

Current ILK system

Voltage ILK system

Ground

- -

Underground

NC magnet

- New interlock will check the voltage of the magnet coil. We plan to implement it to the output terminal of the power supply at the ground floor.
- Is there any noise ?

Preliminary measurement

- Compact system
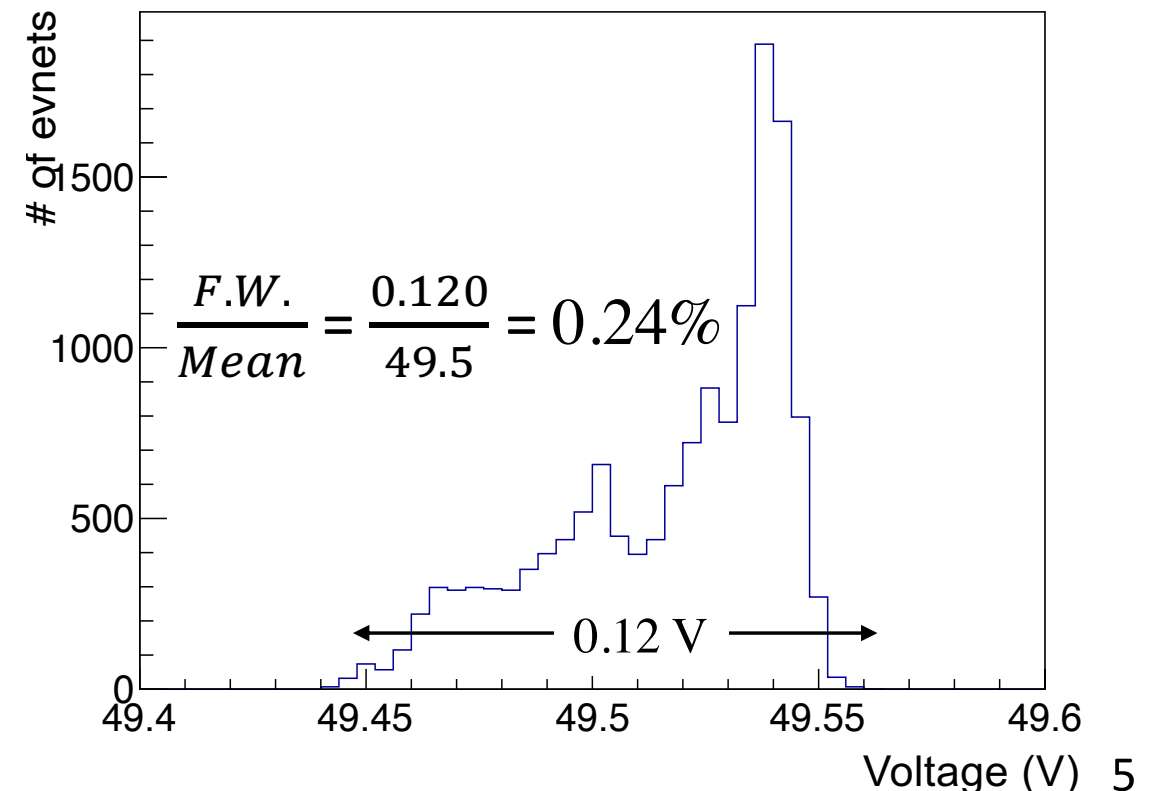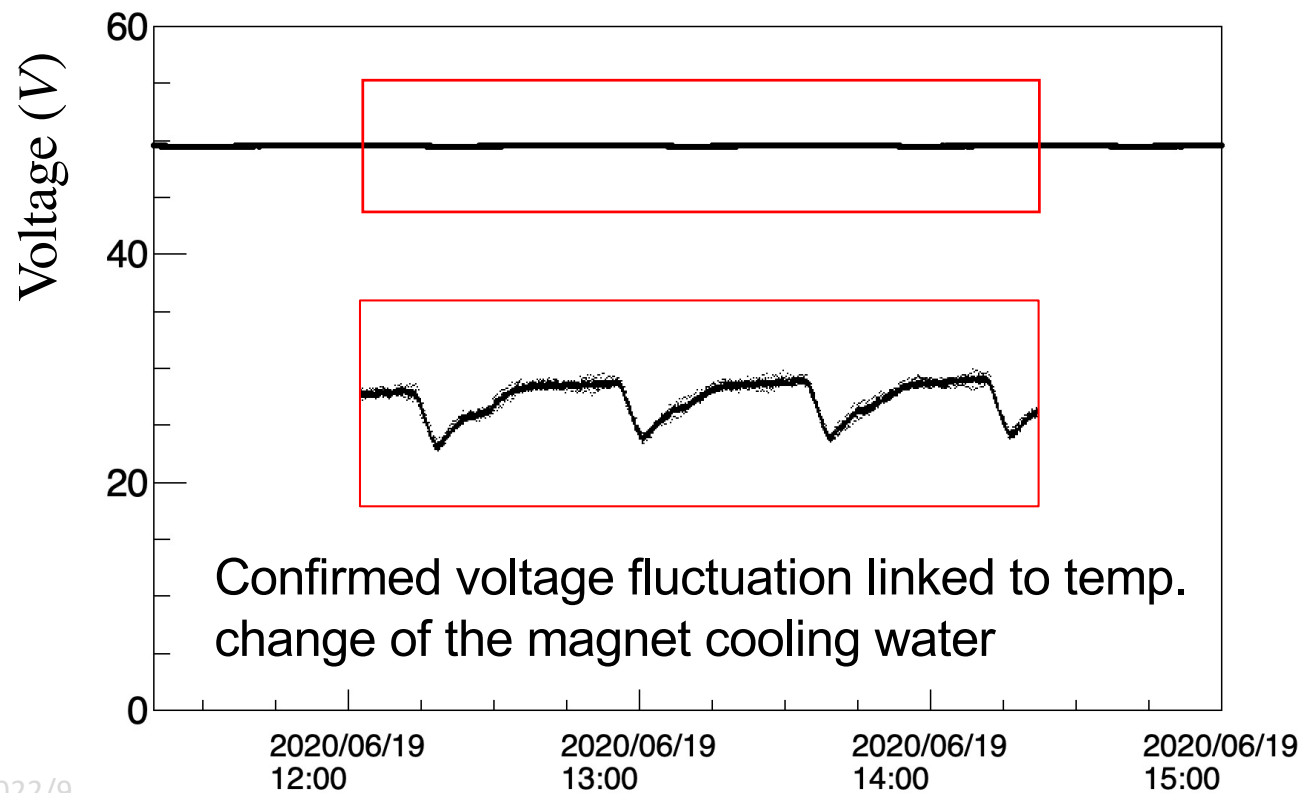- Ease of development
- Intelligent processing

System design

Preliminary measurements

Preliminary measurements were performed to confirm whether
- the voltage of the NC magnet can be measured on the ground floor,
- there is an influence of noise during Main Ring (MR) operation.

In June 2020, while the MR was in operation we confirmed the voltage b/w the output terminals of the PS on the ground floor can be measured with an accuracy of within 1%.

Confirmed voltage fluctuation linked to temp. change of the magnet cooling water

$$\frac{F.W.}{Mean} = \frac{0.120}{49.5} = 0.24\%$$

0.12 V

System design

We considered three candidates of system configurations :
- PLC
- microcomputer + digitizer (ADC)
- FPGA + ADC

In term of latency, ADC performance, ease of development, intelligent processing and cost, a **microcomputer** and a **ADC** are adopted.   This is the first attempt to use these in our interlock system.

Arduino UNO and Pmod-type ADC were used to verify the validity of using a microcomputer and ADC

Validation of the use of Arduino + Pmod-ADC

We have verified the following validity of adopting Arduino + Pmod-ADC.

- **Check feasibility of ADC readout by Arduino with SPI[1]**
- **Check the ability to compare read data with thresholds**
- **Implementation of threshold setting using interrupts**
- **Confirmation the signal can be output as an interlock**
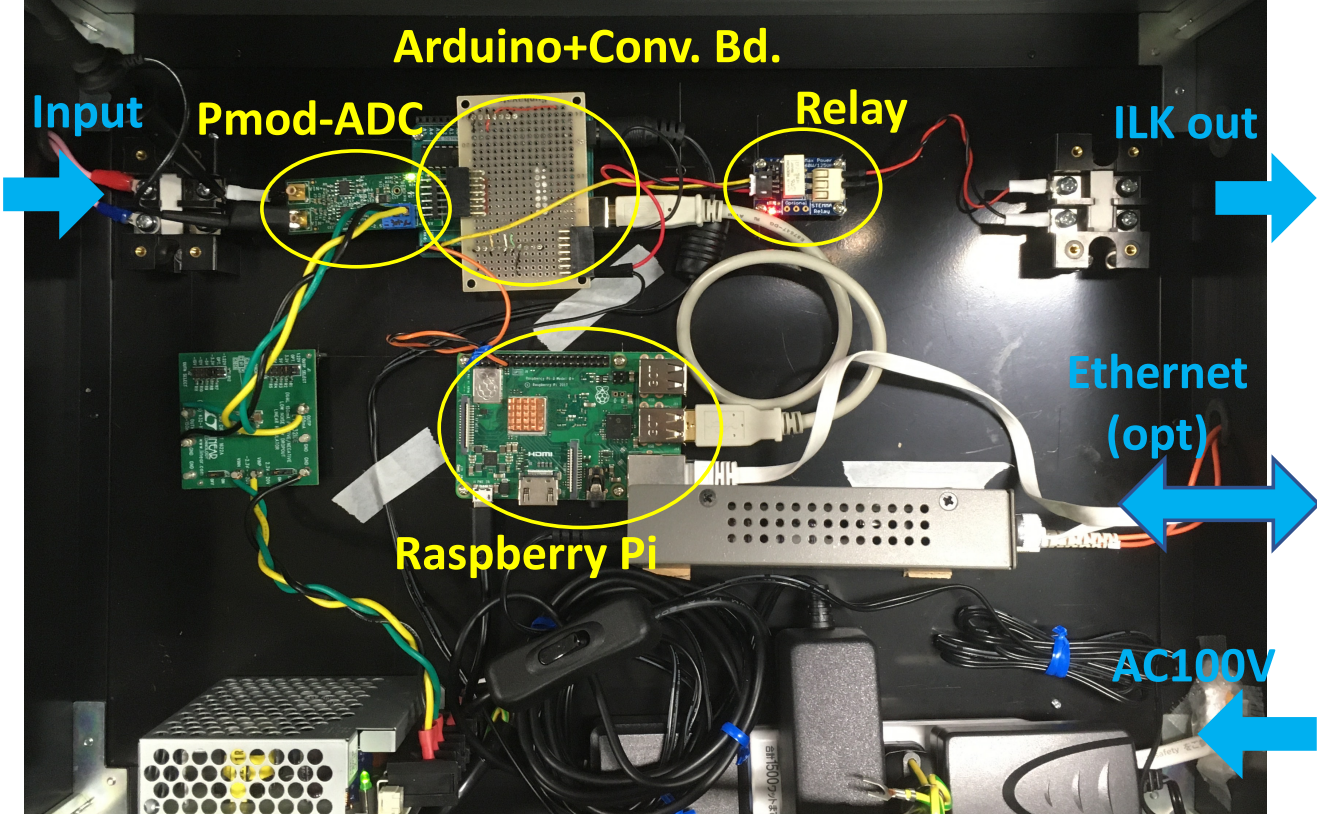
[1]: *Serial Peripheral Interface*
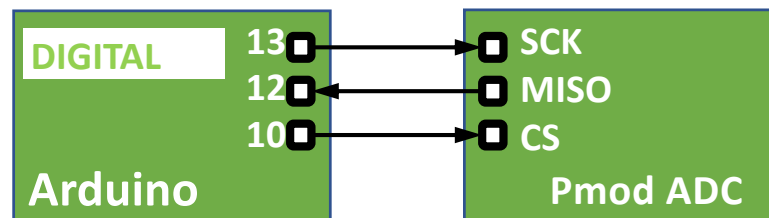
Arduino and Pmod ADC wiring for SPI

Voltage interlock system using Arduino and Pmod-ADC seems to be feasible.

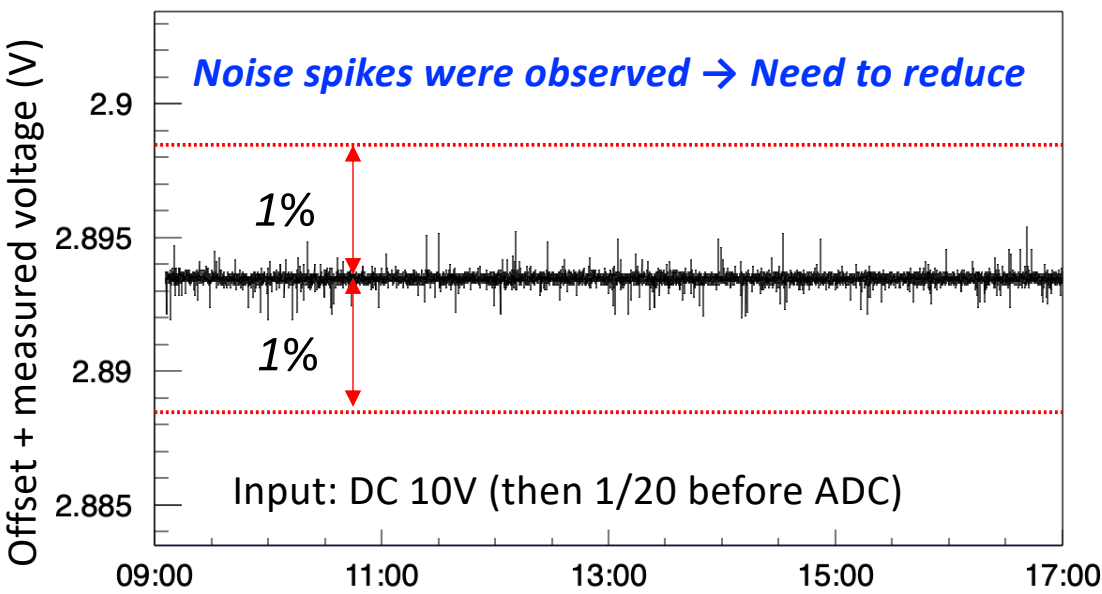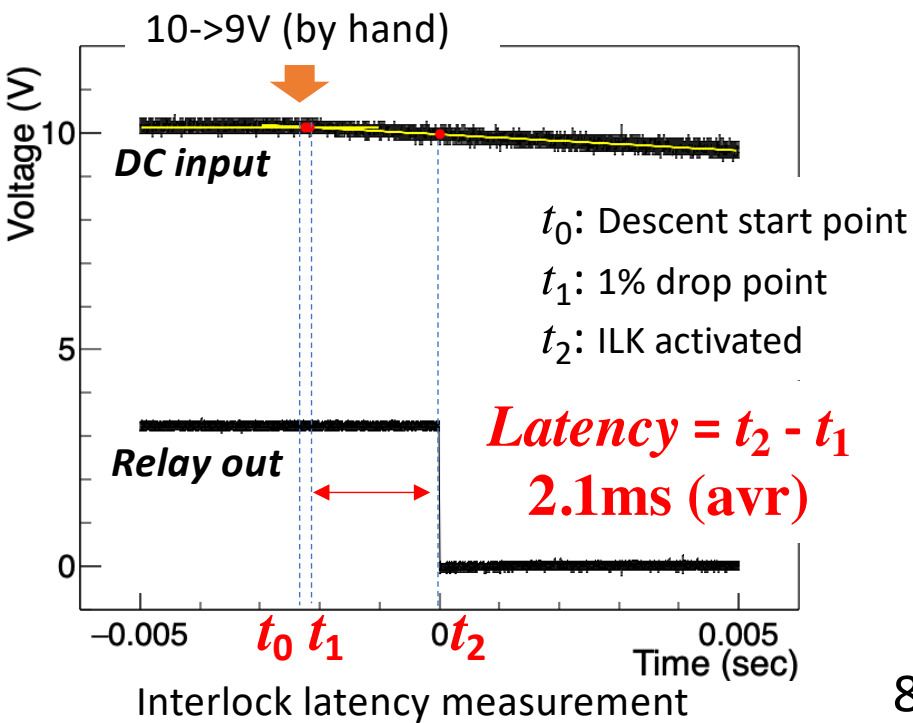Sampling read results

ADC linearity check
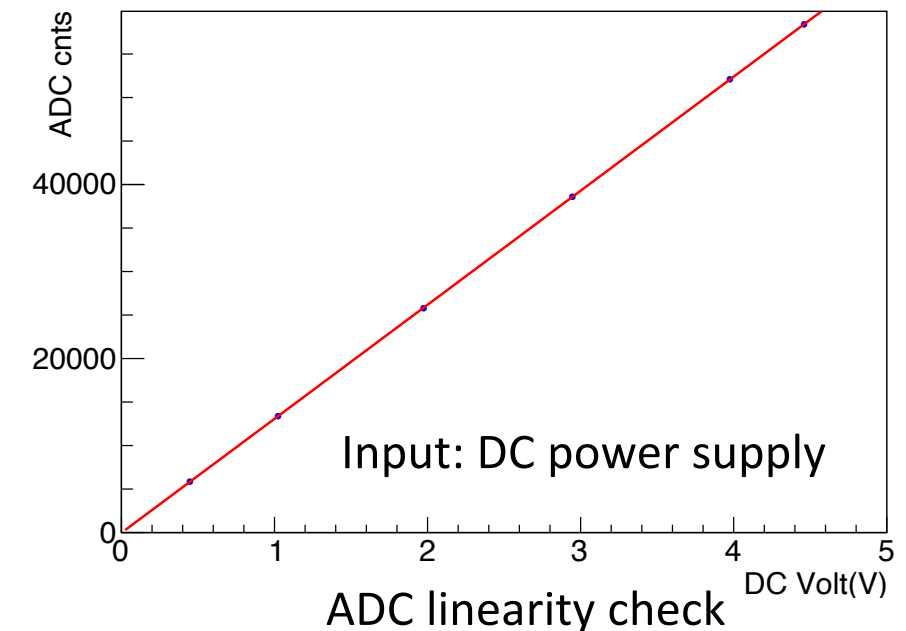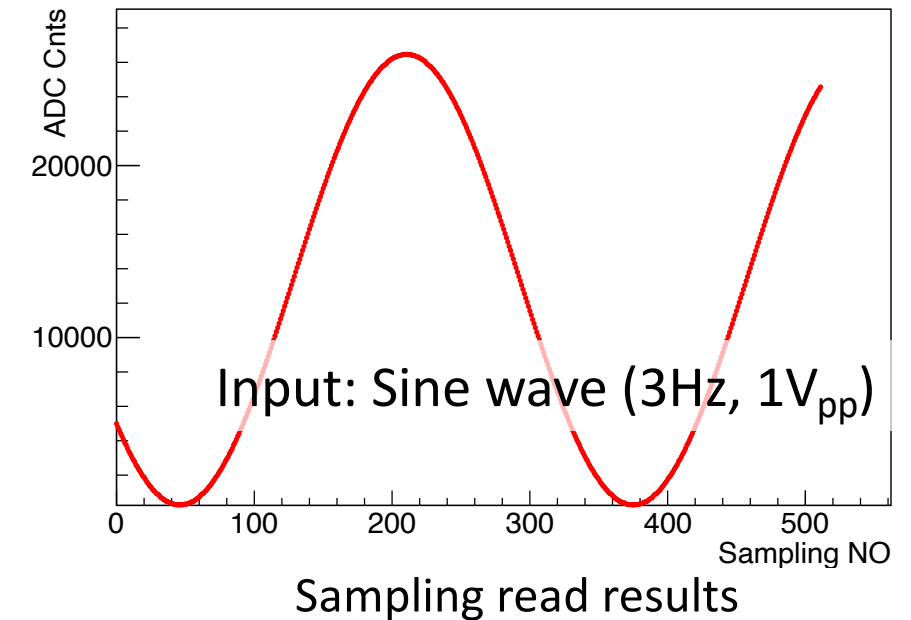
Prototype development and evaluation

We performed long-term stability tests and interlock latency measurements using the prototype.

The prototype in a box

Noise spikes were observed → Need to reduce

1%

1%

Input: DC 10V (then 1/20 before ADC)

Result of long-term stability test

10->9V (by hand)

DC input

t_0: Descent start point
t_1: 1% drop point
t_2: ILK activated

Relay out

Latency = t_2 - t_1
2.1ms (avr)

t_0 t_1 t_2

Interlock latency measurement

ADC board development

After evaluating the prototype, we started developing an ADC board to be used in a real system.
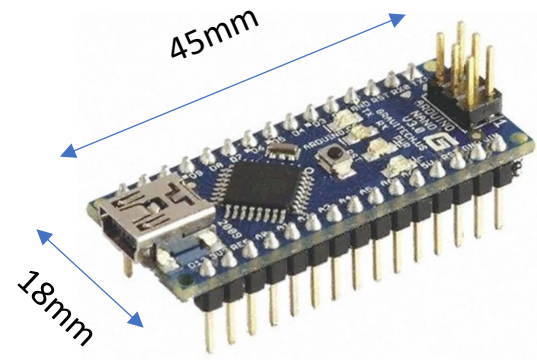
Two types of step-down circuits will be mounted on the ADC boards.

- **Voltage divider circuit (conventional)**
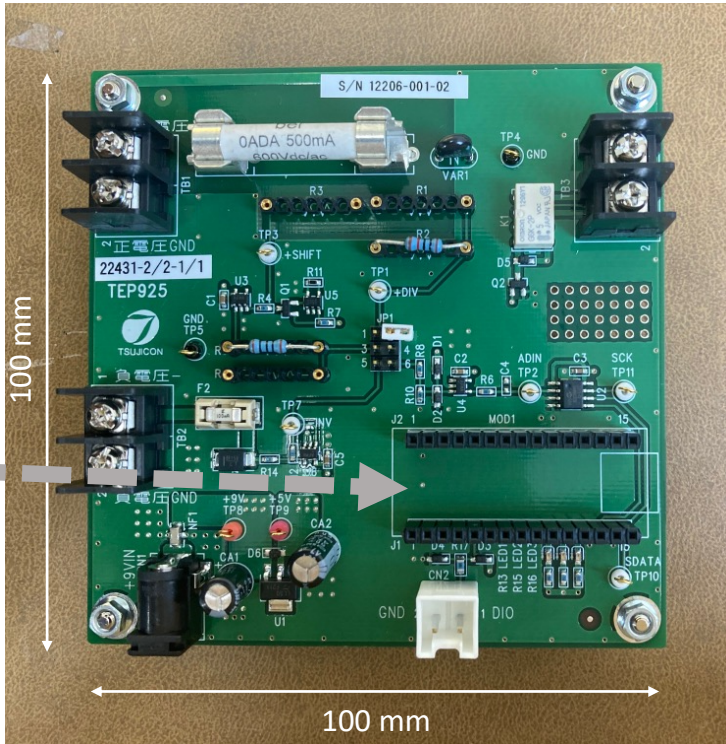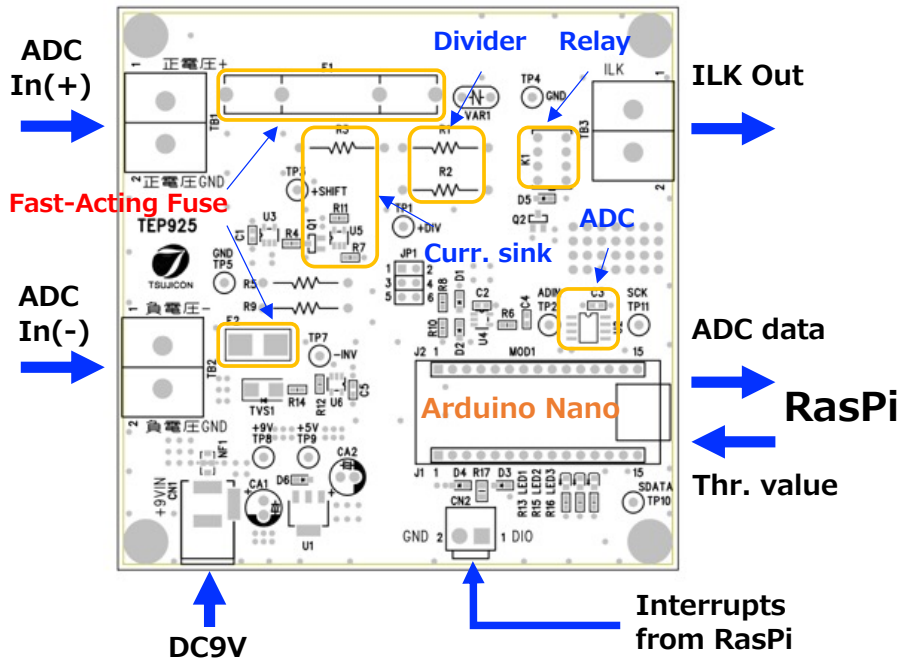- **Constant current sink circuit (*new*)**

We will select one of the above two methods and implement it on the actual board.

ADC：MCP3201
Resolution：12bit
Sample rate：100kSPS
Interface：SPI

45mm

18mm

Arduino Nano

100 mm

100 mm

Evaluation of the ADC board

Evaluation of the voltage divider circuit

☑ ADC data read by Arduino Nano

☑ Data transfer b/w Arduino and Ras. Pi via serial comm.

☑ ADC data acquisition at 1kSPS with 1/2 voltage div. ratio

   Confirmed by inputting sine waves (3Hz, 10Hz, 30Hz)

☑ ADC linearity check

   The output of the OpAmp before the ADC was saturated

☑ The ADC board has no frequency characteristics

☑ The threshold value on Arduino can be changed externally

☑ The output of the interlock signal

Evaluation of the constant current sink circuit

We input the voltage from the sourcemeter to the ADC board and checked the operation of the constant current sink circuit.

Input (V)	Current (mA)	Shift register (Ω)	Shift voltage (V)
8.0 - 16.0	0.990	9.99k	9.89
20.0 - 25.8	0.990	21.98k	21.76
31.0 - 25.8	0.990	33.19k	32.86
45.0 - 50.8	0.990	47.2k	46.73

ADC board and sourcemeter

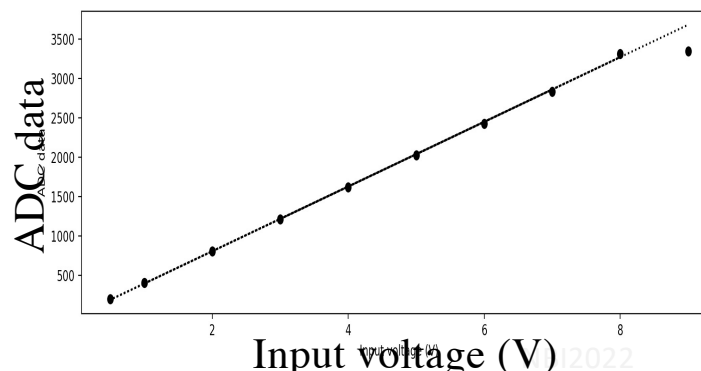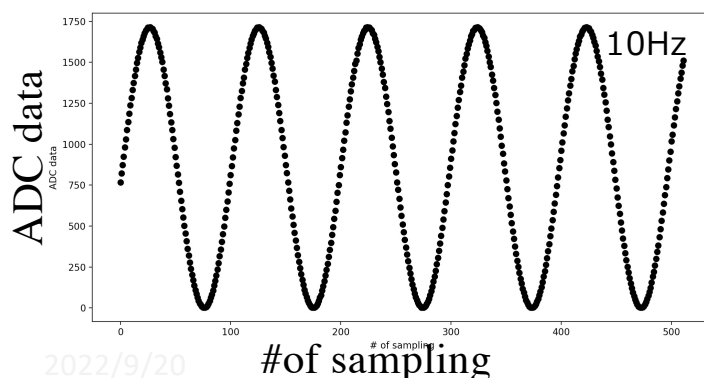# Evaluation of the ADC board

Evaluation of the voltage divider circuit

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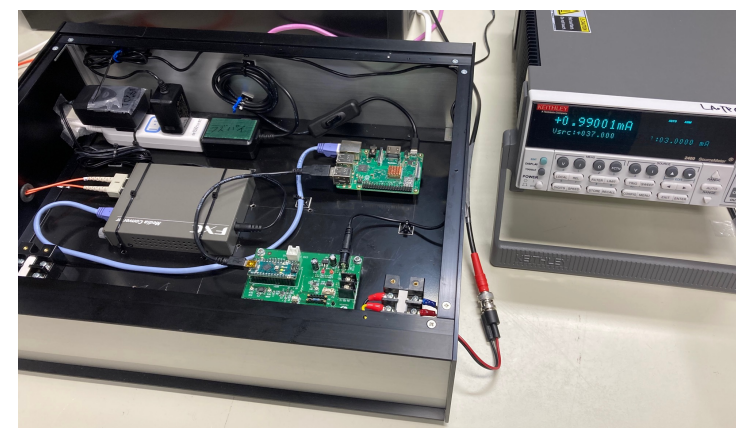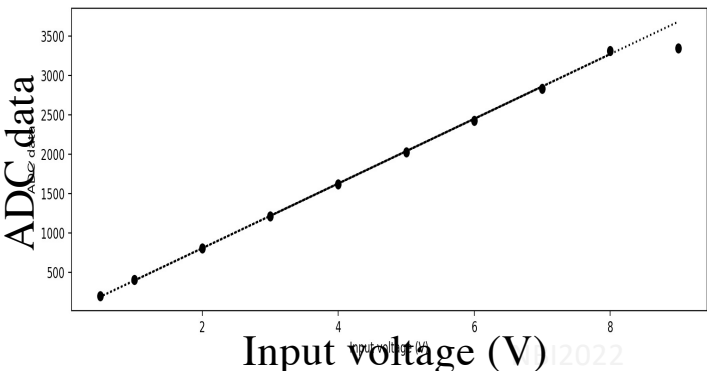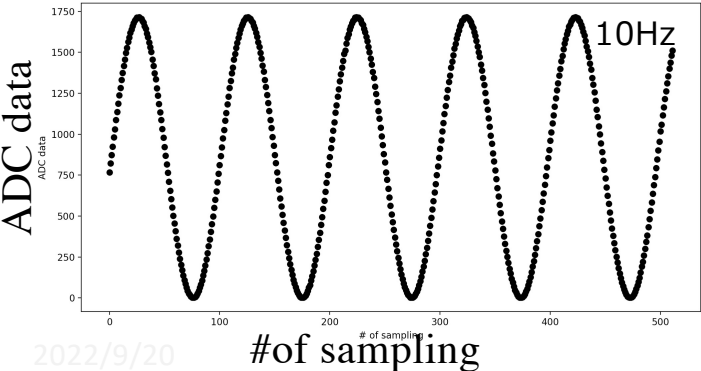☑ ADC linearity check

   The output of the OpAmp before the A~~~

☑ The ADC board

☑ Th~~~~~~~~~~~~ be changed externally

☑ Th~~~~~~~ the interlock signal

Evaluation of the constant current sink circuit

   We input the voltage from the sourcemeter to the ADC board and checked the operation of the constant current sink circuit.

Input (V)	Current	S~~~~~	~~~te
			9.89
		21.98k	21.76
~1.0 - 25.8	0.990	33.19k	32.86
45.0 - 50.8	0.990	47.2k	46.73

No major problems have been found

ADC board and sourcemeter

Future plan

As for future plans, after evaluating the ADC board, we plan to conduct a test under actual load and proceed with a comprehensive evaluation including long-term stability before starting operation.

Preliminary measurements

System Design

Prototype development and evaluation

ADC board development and evaluation

Implementation and performance evaluation

Done

Doing

Not yet
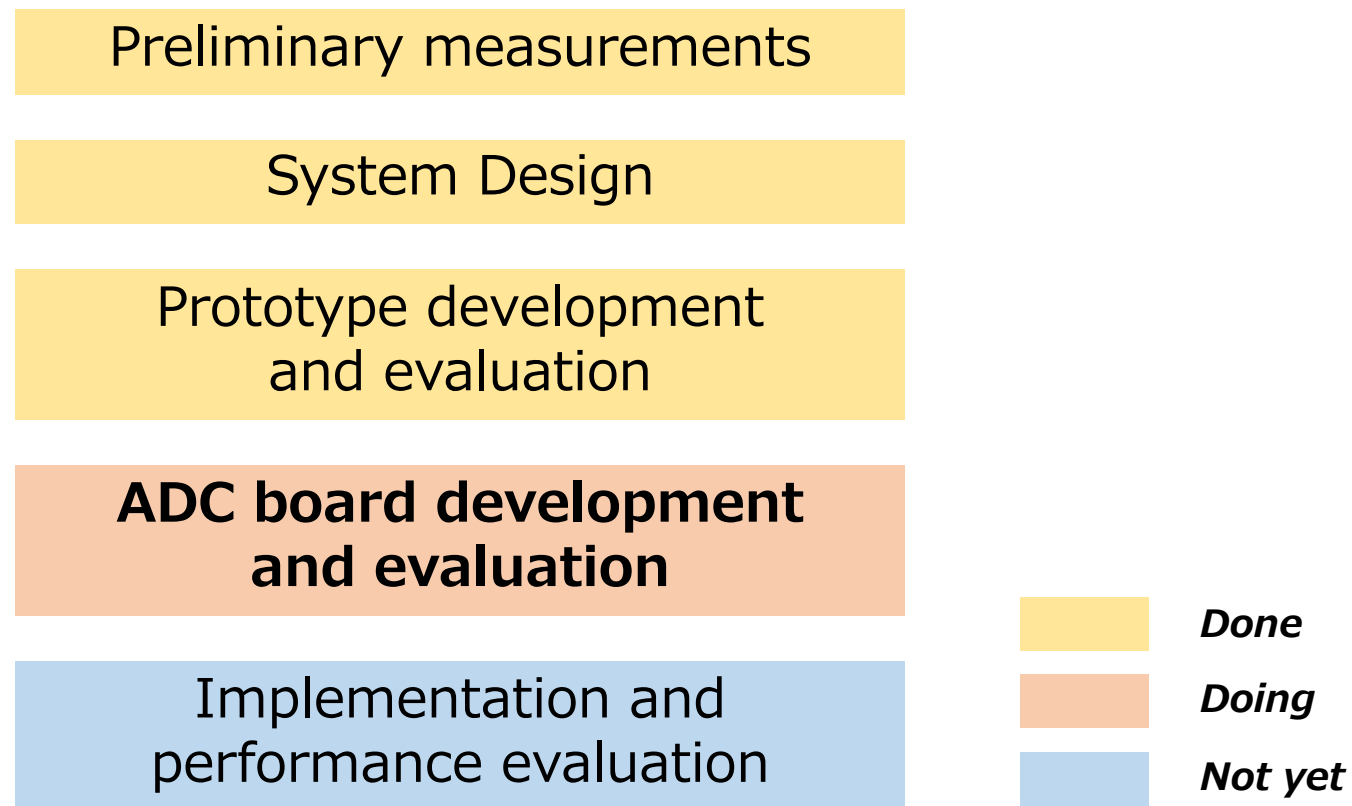
Summary

- J-PARC Neutrino experimental facility is upgrading its beamline to achieve a beam power of 1.3MW. One of those items is an interlock enhancement.
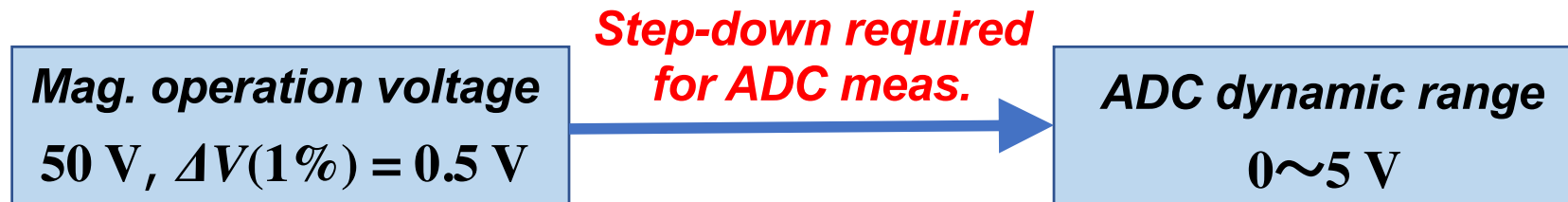
- In order to detect magnet coils troubles we are implementing a new mode into the interlock system on normal-conducting magnet.

- We realized the ease of system development and expandability by using a microcomputer in the system. We developed and evaluated a prototype and confirmed that it satisfies the required performance (accuracy: 0.12%, MPS latency time: 2.1ms).

- Currently, we are developing an ADC board with a microcomputer to be used in the actual system.   ADC board prototypes have been completed and is being evaluated. No major problems have been found at this time.

- We plan to conduct a test under actual load and proceed with a comprehensive evaluation including long-term stability before starting operation.

Backup

"*Resistor divider*" or "*Const. current sink*"?

Mag. operation voltage 50 V, $\Delta V(1\%) = 0.5$ V	**Step-down required for ADC meas.** →	ADC dynamic range 0～5 V

A key issue in ADC board evaluation is the step-down method selection.

	Resistor divider	**Const. current sink**
Circuit	**Simple**	Requires shunt regulator IC and transistor
Sensitivity	Detects 1/N of voltage fluctuation	**Fluctuations can be measured directly**
Input signal S/N	Not good	**Good**
Applicable voltage	**All range of operating voltage**	Part of the operating voltage range
Experienced	**Yes**	No

We are evaluating the two methods of ADC boards and decide which one to implement in the actual system.