Contribution ID: 20 Type: Standard Talk

Data acquisition and processing for Zynq UltraScale+ based AMCs using high-level synthesis languages

Tuesday, 8 April 2025 09:20 (20 minutes)

This contribution presents a data acquisition and processing system implemented for a MicroTCA Advanced Mezzanine Card (AMC) that is based on an AMD Zynq UltraScale+ MPSoC. The presentation focuses on the methodology to develop custom applications on such system,

The hardware implemented into the FPGA includes the JESD204B high-speed ADC/DAC interface, as well as PCIe connectivity for data streaming to/from external systems. Furthermore, it supports high-level synthesis languages like OpenCL and HLS, reducing the development time of data acquisition and processing algorithms compared to traditional hardware description languages.

In addition, an embedded Linux is deployed using Yocto-based tools to run on the Zynq ARM cores. This enables efficient heterogeneous processing, where control and management tasks run on the processor while computationally intensive operations are offloaded to the FPGA.

The presentation focuses on the application development methodology for the system, highlighting how standard drivers and API simplify its development and maintenance.

Finally, a use case is presented in which the system is used to implement and verify a digital pulse shape analysis algorithm for signals acquired at 1GSamples/s.

Primary authors: PIÑAS, Alejandro (UPM); Dr CARPEÑO, Antonio (UPM); Mr GONZÁLEZ, César (UPM); Dr

RUIZ, Mariano (UPM)

Presenter: PIÑAS, Alejandro (UPM)

Session Classification: EPICS Plenary Session

Track Classification: Hardware and Hardware Interfaces