Ion implantation Ion Sources in Semiconductor Fabrication: source life, beam stability, defects, yield improvements and contamination control

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AGENDA

- Evolution of Ion sources in Ion Implantation
- Dopant Plasma Chemistry
- Ion Beam Sputtering and Metal Contamination
- Particle Transports and Loss of Device Yields
- Summary

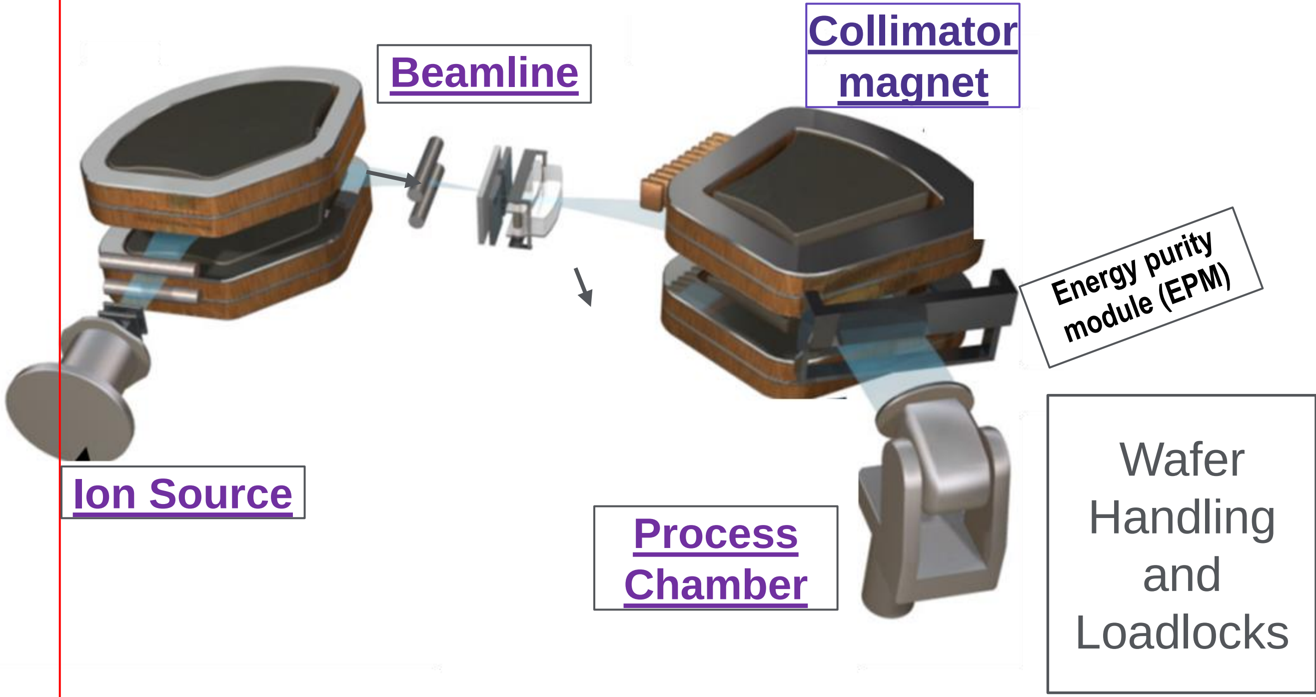
Ion Implant & Ion Source Requirements

Throughput
- **Fast transitions between beam recipes <3min**
- **High productivity (up to 500 wafers per hour)**

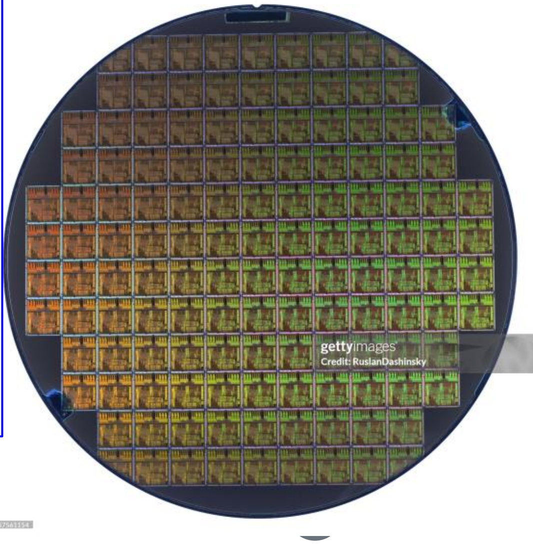
Cost of ownership
- **Long ion source lifetime >300 hrs**
- Availability (“uptime”): >95 %

Process integrity
- **Beam Glitches: low & controlled**
- **Low metal contamination (essential for Advanced Nodes and CMOS Image Sensors)**
- **Low particles on wafer**
- **Dose uniformity: < 0.5 %, one sigma**
- **Dose repeatability: < 0.5 %, one sigma, wafer-to-wafer, day-to-day**
- Beam angle: horizontal/vertical < 1°
- Energy purity

Items in bold drive ion source design



Ion Source : Generates ions for implant
AMU Mag: Filters incoming ions by desired mass/charge ratio
Beamline: Focuses and transports beam
Collimator magnet: Final bend and makes beamlets parallel
EPM: Vertical deflection for energetic neutral control
Process Chamber: Wafer is implanted



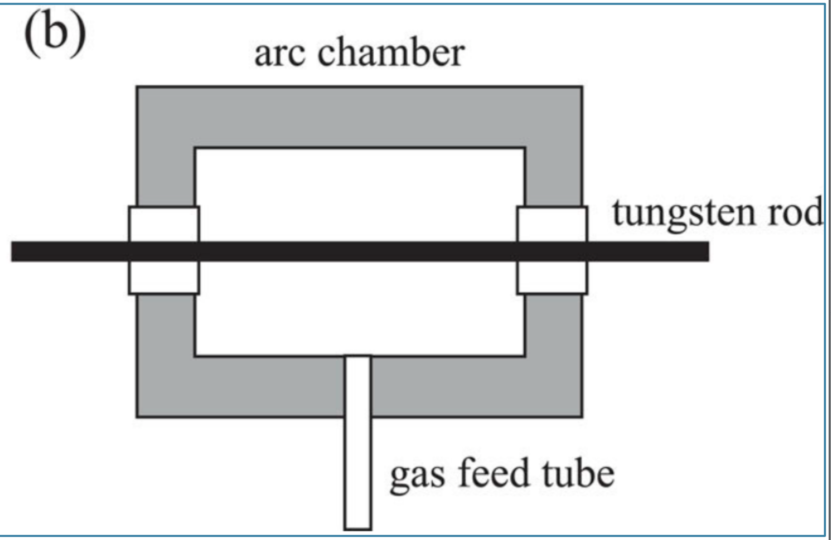
Ion sources (Freeman → Bernas → IHC)

- Improved source lifetime
- Better reliability
- Reduced contamination

Three ion implant tool types:

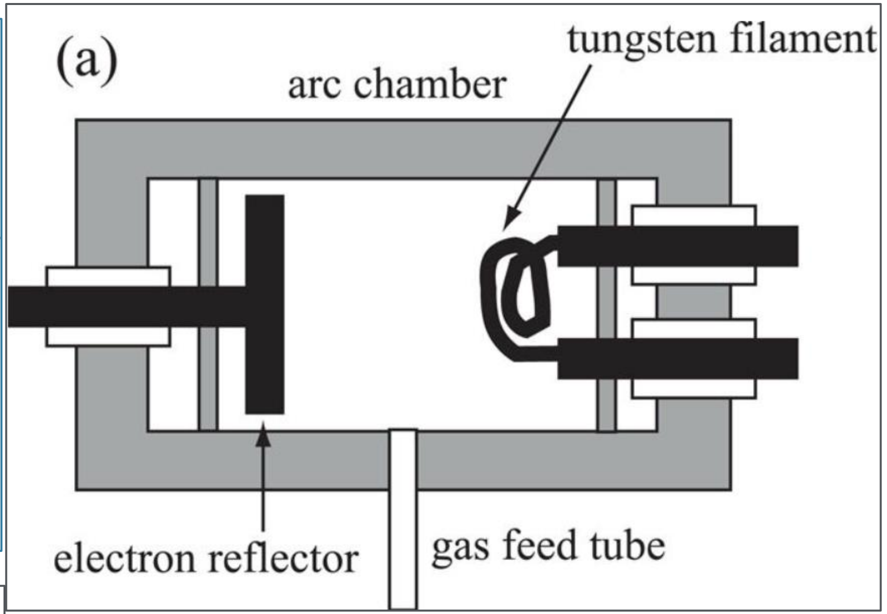
- Medium Current: 10^{11}-10^{14} ions/cm^2, 300keV(+)
- High Current: 10^{13}-10^{16} ions/cm^2, 60keV
- High Energy: 10^{10}-10^{13} ions/cm^2, >1 MeV

Freeman Source



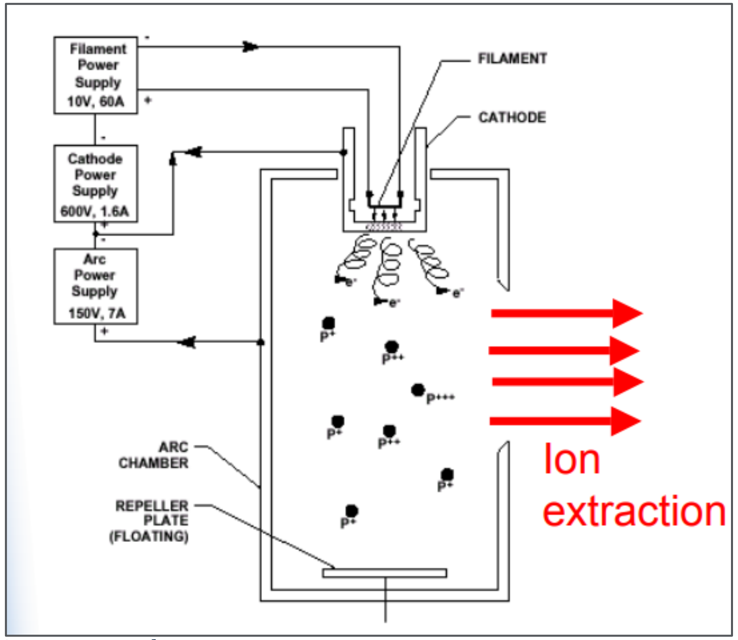
D. J. Chivers, 1992, **Freeman ion source: An overview (invited);** *Rev. Sci. Instrum.* 63, 2501–2506 (1992)

Bernas Source

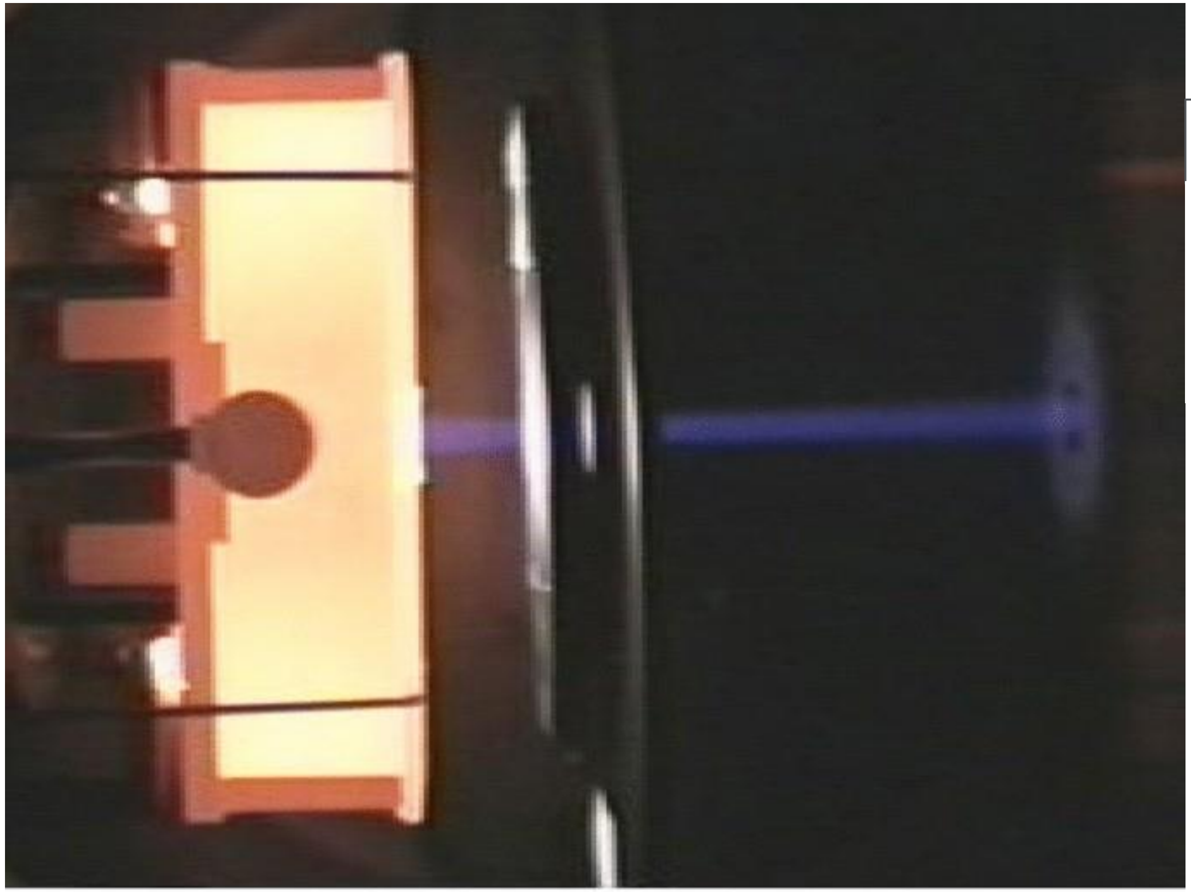


Ian G. Brown, Editor, 2004, The Physics and Technology of Ion sources, Chapter 8, Marvin Farley, Peter Rose, Geoffrey Ryding, The Physics and Technology of Ion Sources, 2nd Edition; Wiley-VCH Verlag GmbH & Co. KGaA

IHC Source



Indirect Heated Cathode(IHC) Ion Source



An R&D moment. Taken during the development of an IHC source

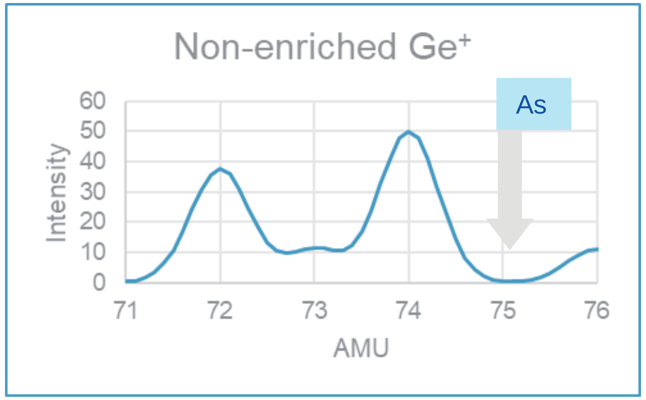
Anthony Renau,"35 Years of challenge and innovation in ion implant," in *MRS Advances*, volume 7, in 2022.

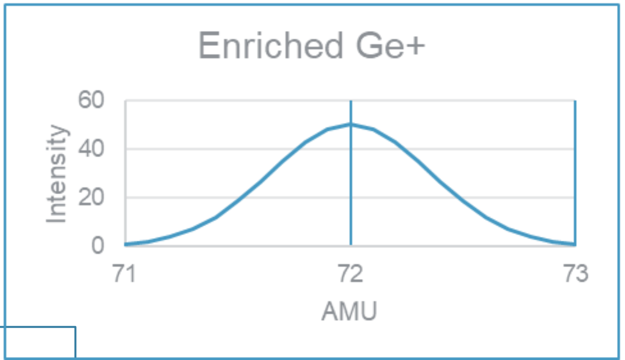
Typical species used for semiconductor implanters

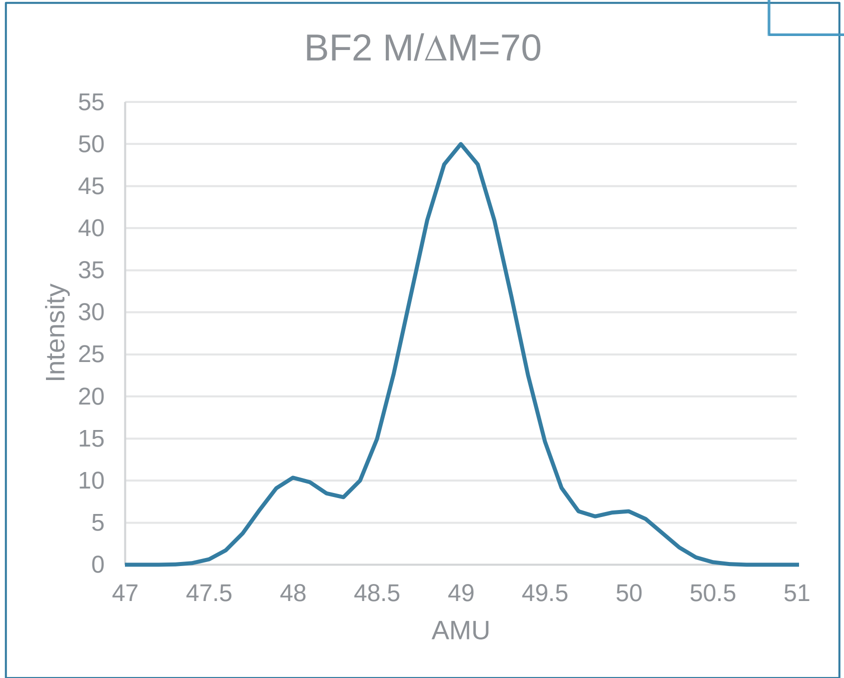
N-type	P, As, Sb
P-type	B, BF2, Al, Ga, In
Non dopant	H, He, C, N, F, Si, Ar, Ge, Xe

Implant process requires species purity

- Elements present in ion source components, or deposited on walls become ionized and can be transported down beamline
- Analyzer magnet (mass resolution M/ΔM) can eliminate many contaminants
- Isotopically enriched feed gas is also used to avoid mass coincidence
- Most famous direct mass coincidence:
  - **BF_2^+** (AMU = 48, 49) beams by **Mo^{++}** ion isotopes ($\frac{AMU}{q}$ = 47.5, 48, 48.5, 49, 50, q=2)
  - Avoid Mo in source for BF_2^+







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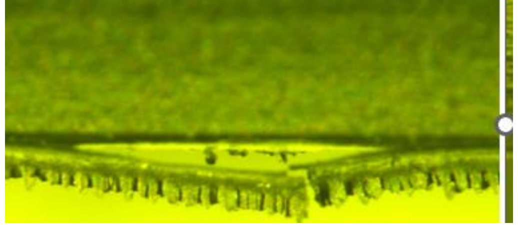
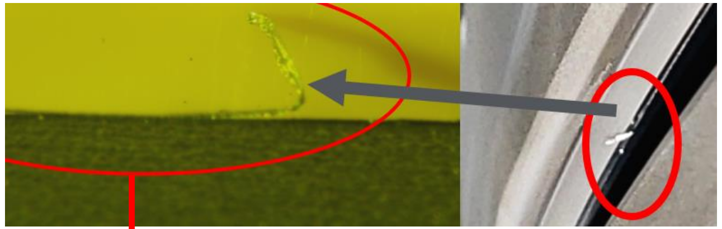
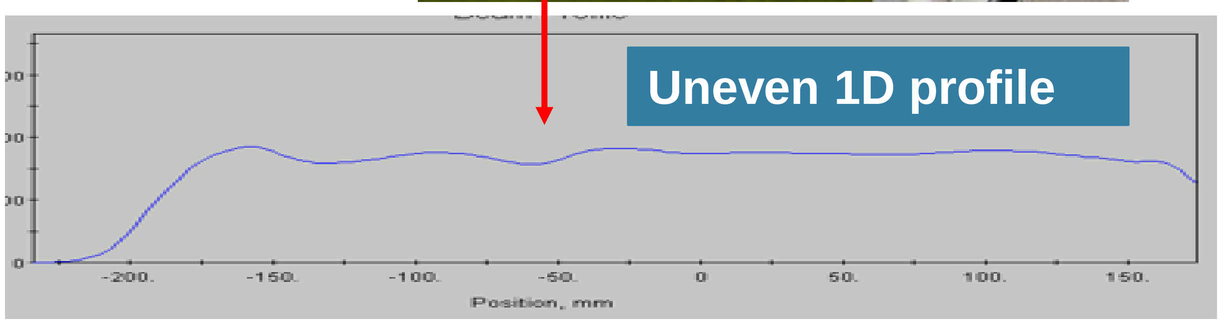
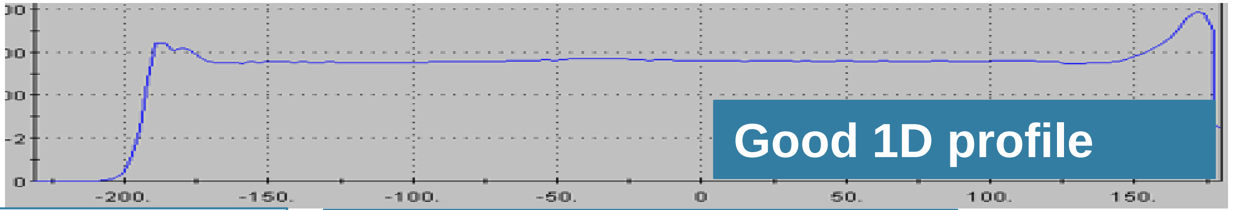
Tungsten – Halogen Cycle

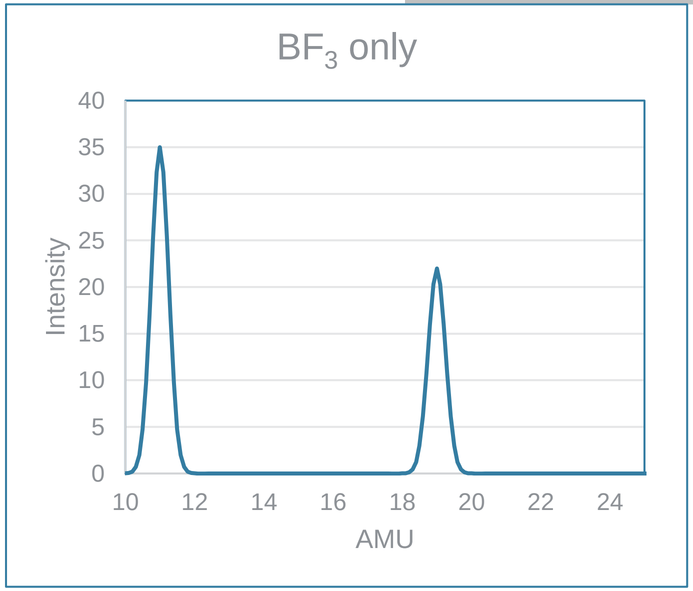
- Most ion sources are composed of tungsten for high temperature environment
- When running fluorine-containing gasses (BF_3, GeF_4, SiF_4), fluorine etches and redeposits tungsten on hot surfaces
- Tungsten etching and buildup can limit source life
  - » Cathode punch through
  - » Repeller growth
  - » Deposition on extraction aperture
- Addition of H_2 gas ties up halogens and limits tungsten halogen cycle

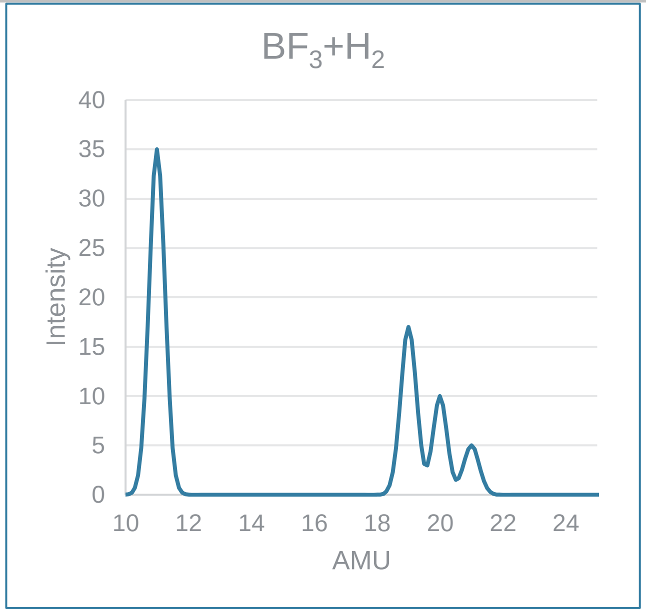








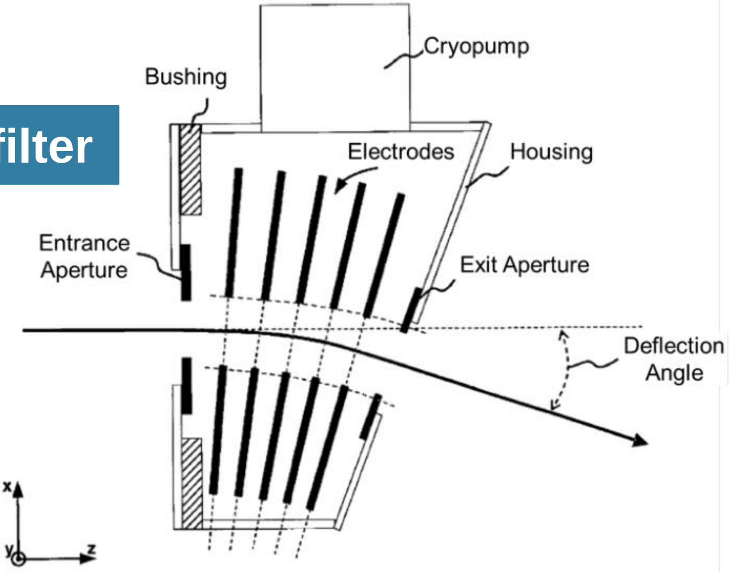


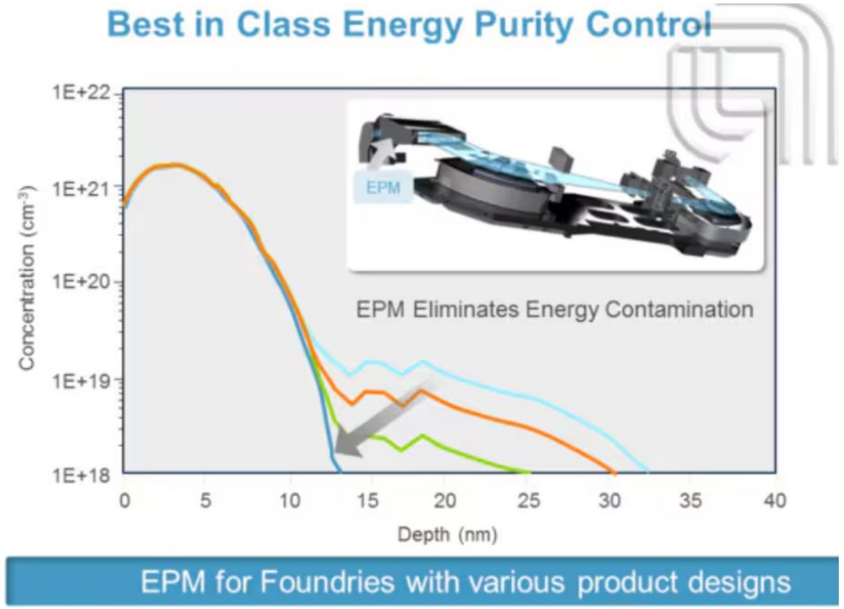


Beam Energy Purity

- To efficiently deliver high currents of low energy beams, the **Applied Materials ® Trident™** Implanter extracts beam at high energy, e.g. 33keV
  - This allows optimal transport through ~3m long beamline
- Just prior to implantation the beam is decelerated to low energy, e.g. 3keV
- Any ions neutralized upstream of the decel, would be implanted at full transport energy, resulting in incorrect implantation depth
- The **Trident™** implanter employs a Energy Purity Module, which decelerates and deflects the ions, thereby filtering out any high energy neutrals before they can hit the wafer

EPM filter





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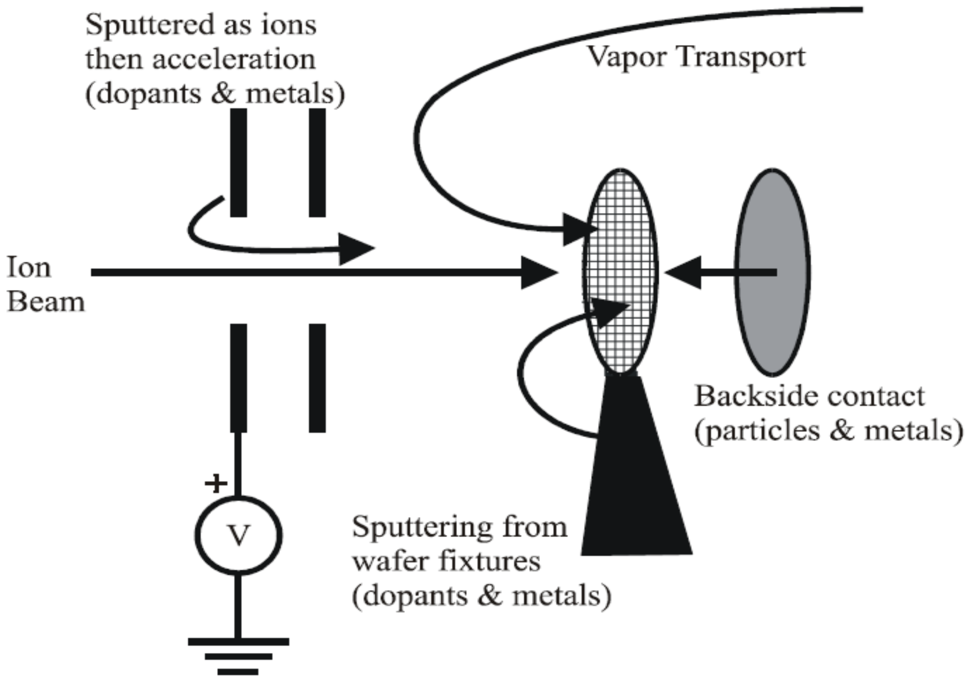
Wafer Metals Contamination



Cartoon of major pathways for contaminants to an ion implanted wafer including (1) multiple ion types in the direct ion beam, (2) various forms of sputtered dopants and metals from accelerator and wafer holding fixtures, (3) vapor transport of dopants and (4) transfer from contact with heat sinks and other wafer holders.

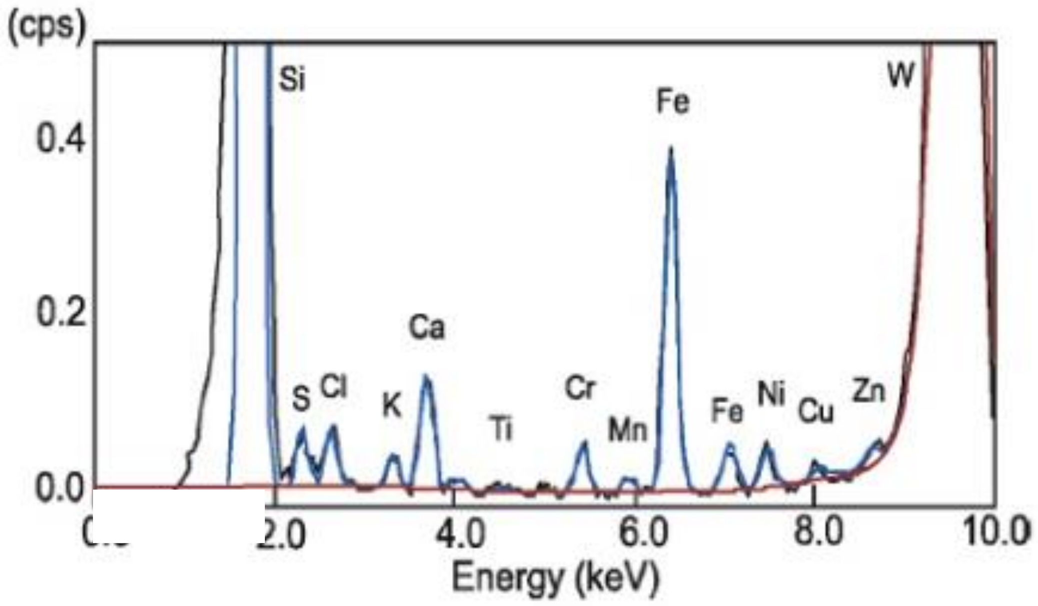
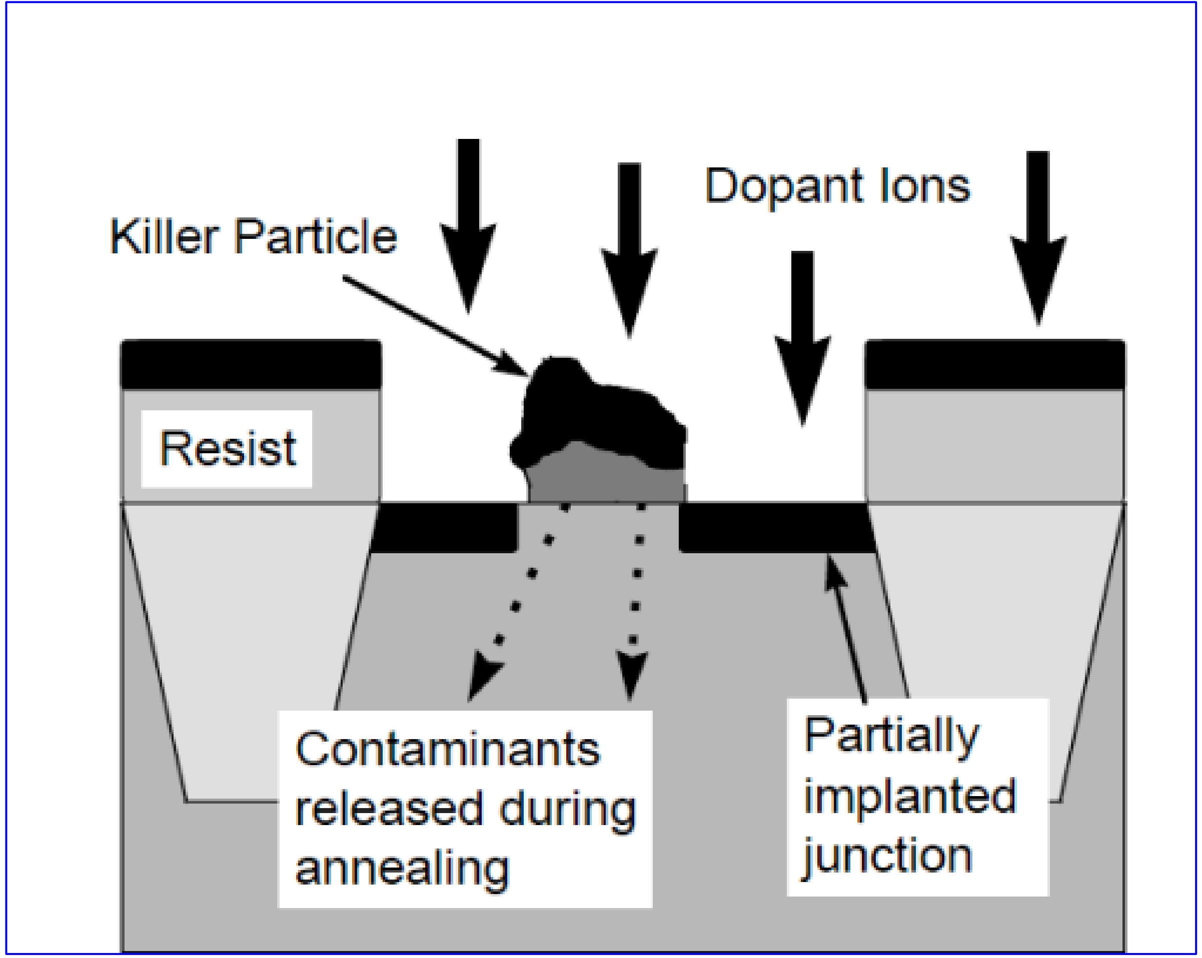


Figure 1 TXRF spectrum of metallic impurities on Si wafer

M. Current, Ion Beam Purity and Wafer Contamination: In book: Ion Implantation Technology: Science and Technology-2016

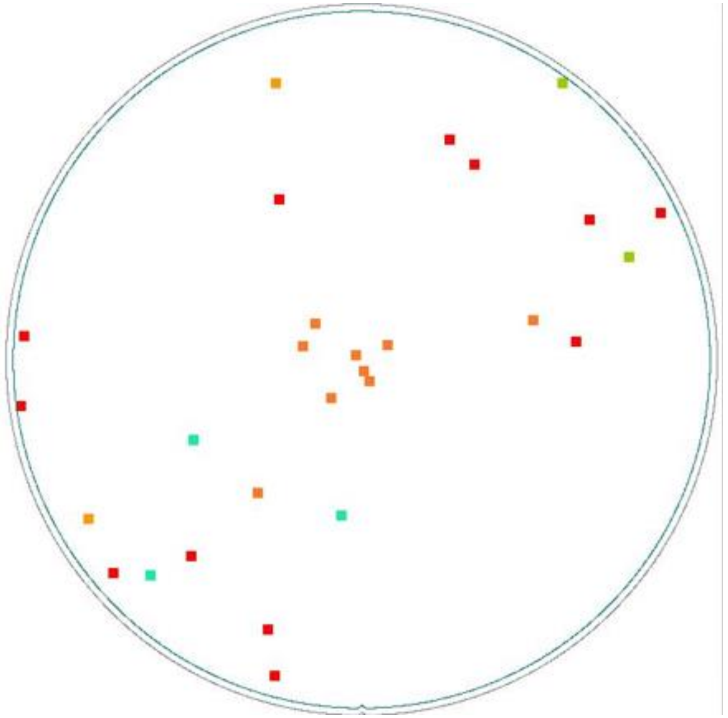
Metal Contamination measured via TXRF and ICP-MS: Standard Metal Tests
Monitor Recipe: Arsenic 40keV_1E16/cm^2
Detection limits: in ~10^8 atoms/cm^2
Metals specification: between 10^9 to 10^{10} atoms/cm^2 for most metals.

Particles are so harmful!



Ion Beam Purity and Wafer Contamination: In book: Ion Implantation Technology: Science and Technology-Sept. 2016

Device masked due to particles

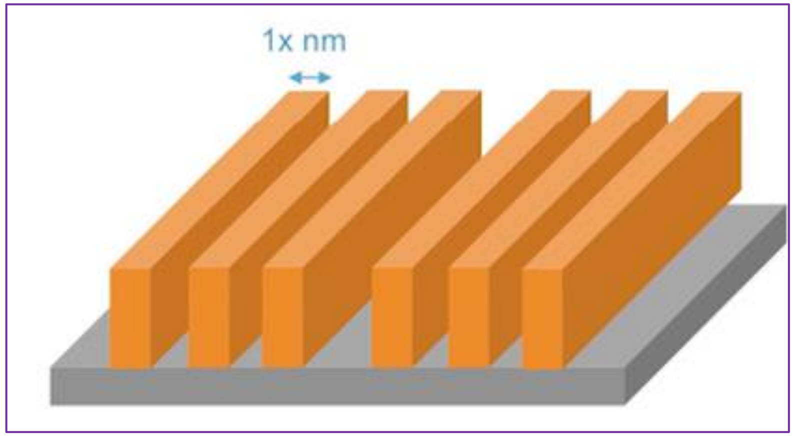


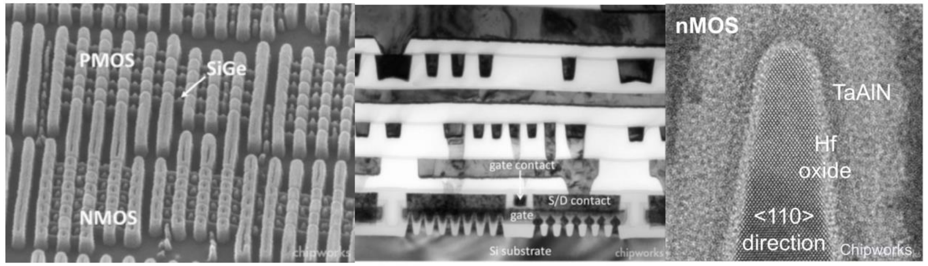
Typical unpatterned particle monitor wafer that contained lots of particles

Device Yield Loss: Particles and Defects

A logic fab with 100,000 Wafer Starts Per Month loses > $$M/yr for every 1% yield loss; Typical yield loss related to defects in High Volume Manufacturing (HVM) 3-5% (Device type related)

More particles mean less $$$

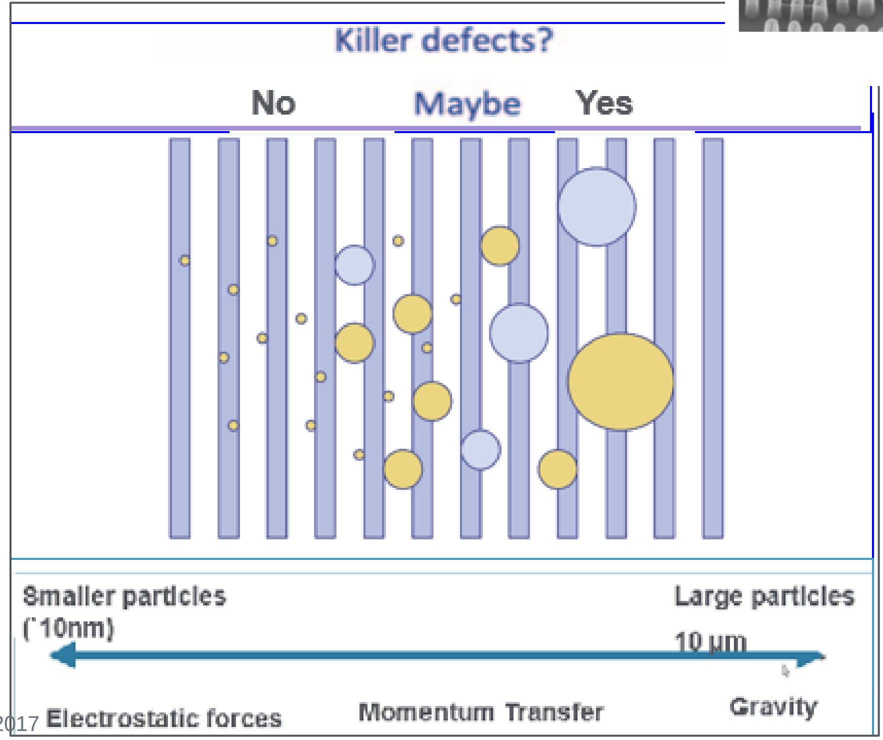


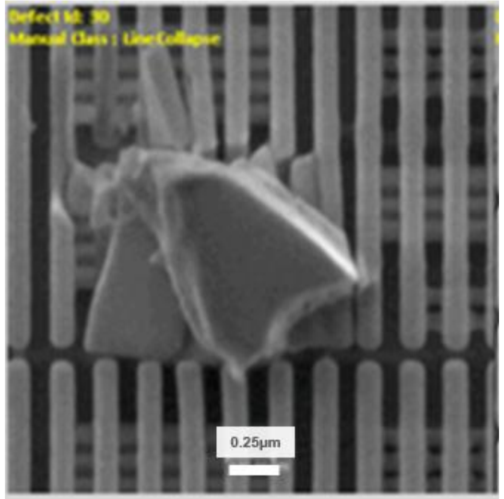


Intel 22 nm FinFET: Images by Chipworks

Sources of Particles:

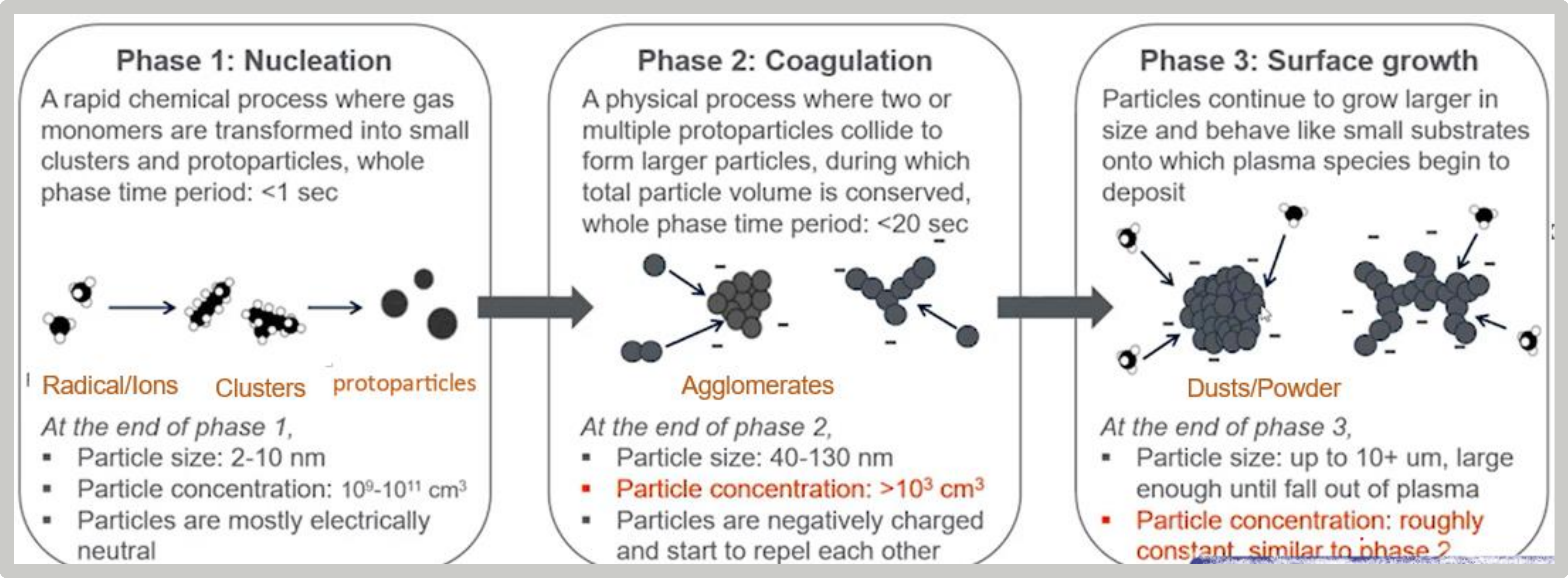
- Debris from arc discharges carried in the ion beam can be transported to the wafer
- Delaminated deposited on surfaces
- Stressed layers (tensile or compressive) have momentum
- Particle forces with charges and velocity altered the particle transport trajectories





In-line Defect

Typical film growth in gas phase under ion beam sputtering

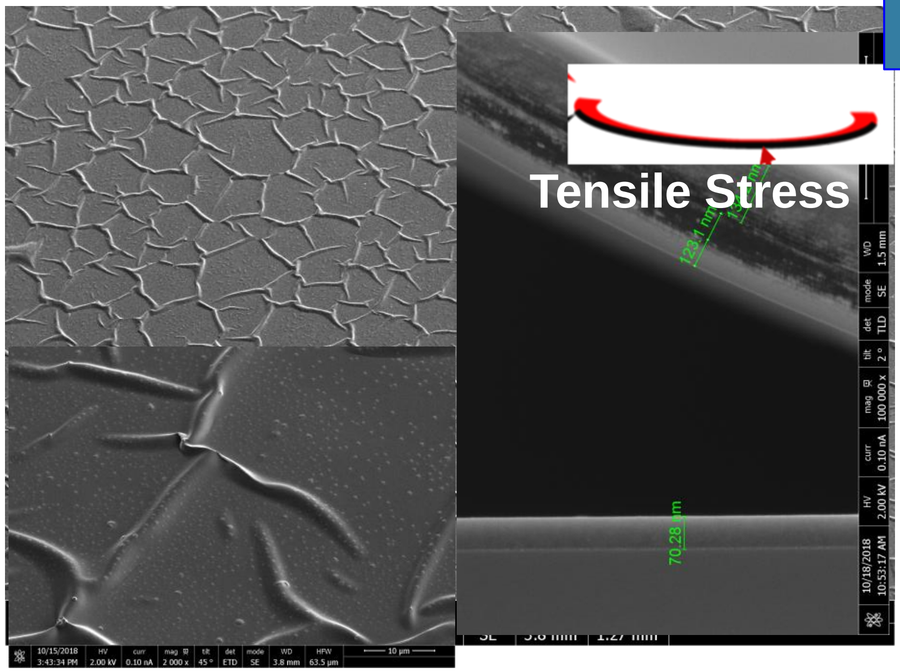


Ion Beam Purity and Wafer Contamination:
•In book: Ion Implantation Technology: Science and Technology-2016
Editors: J. F. Ziegler

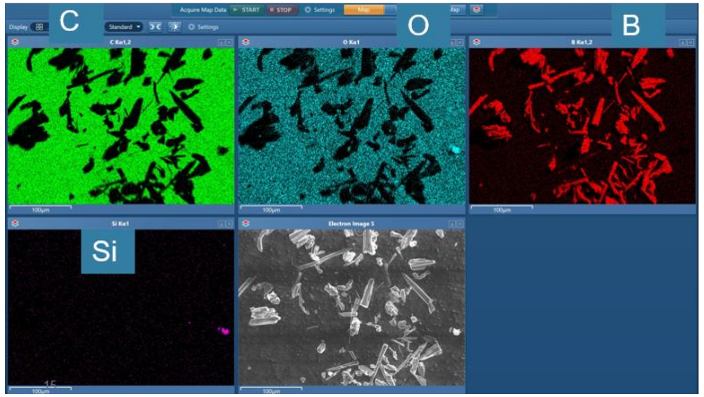
Ion Beam Sputtering and Sources of Particles

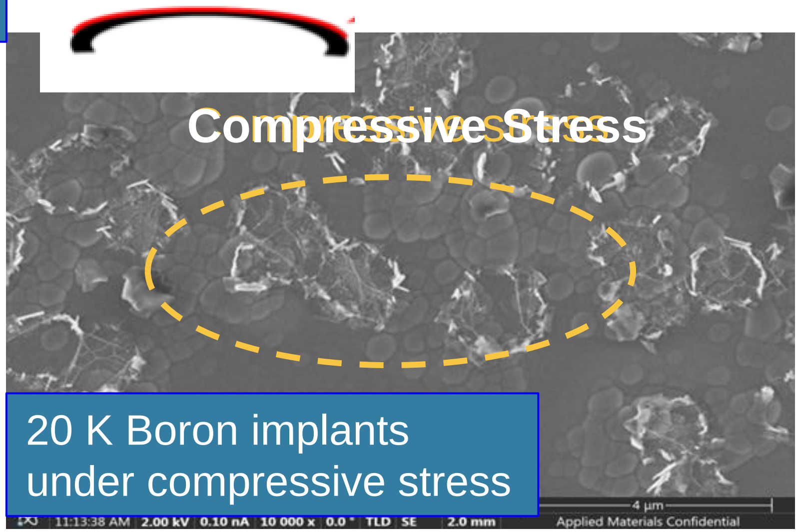
- **Large amounts of accumulated material in the implanter due to sputtering of beamline components**
- **Lots of sputtered materials accumulated forming layers with stresses.**
- **The by-products deposit on surfaces with stored energy as shown below**
- **Delamination of these coatings can result in particles on the wafer**

Deposited film from Phos 3keV implant is highly tensile and caused delamination



Deposited film from Boron 10keV implant with granulated crystals.





20 K Boron implants under compressive stress

Defect Reduction Trend and Particle Forces

measured in Defects per cm^2, defect density targets by node and fab maturity, for logic nodes:

Technology Node (nm)	Target Defect Density @ 300 mm Wafer	Real FSP Adders (Total/Area)	Monitor Defect Sizes(nm)
10 nm	<70-200	20/5	45 nm
7 nm	<35-140	15/5	45 nm
5 nm	< 70	<10/2	45 nm
3 nm	< 35	<5/2	32 nm
2 nm	< 7 to 21	< 4/2	26 nm

[a] Partially converted from SIA Yield Enhancement Report. The values vary by fab and are guarded proprietary data

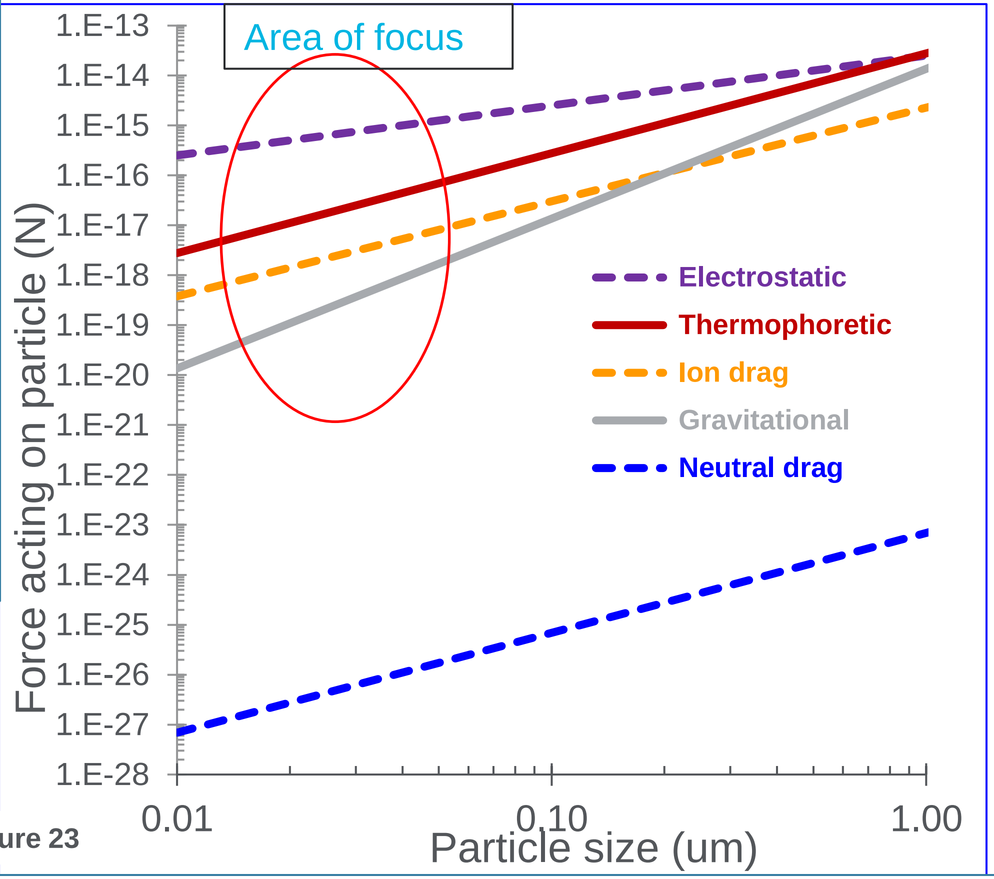


Figure 23

Probability of Transport – Forces on a particle
Wafer adders can be described mathematically:

$$N_{Adders} = N_{Sources} P_{Transport} P_{wafer}$$

Sources – good house keeping
Probability of adder getting to or stopping on the wafer – "weighted" view solid angle

Particle forces are **the electrostatic force, the ion drag force, the neutral drag force, thermophoresis, and gravity.** **They depend on the sizes of particles and charges.**

Ref: J.F. O'Hanlon et al, IEEE Trans. Plasma Science,22,1994

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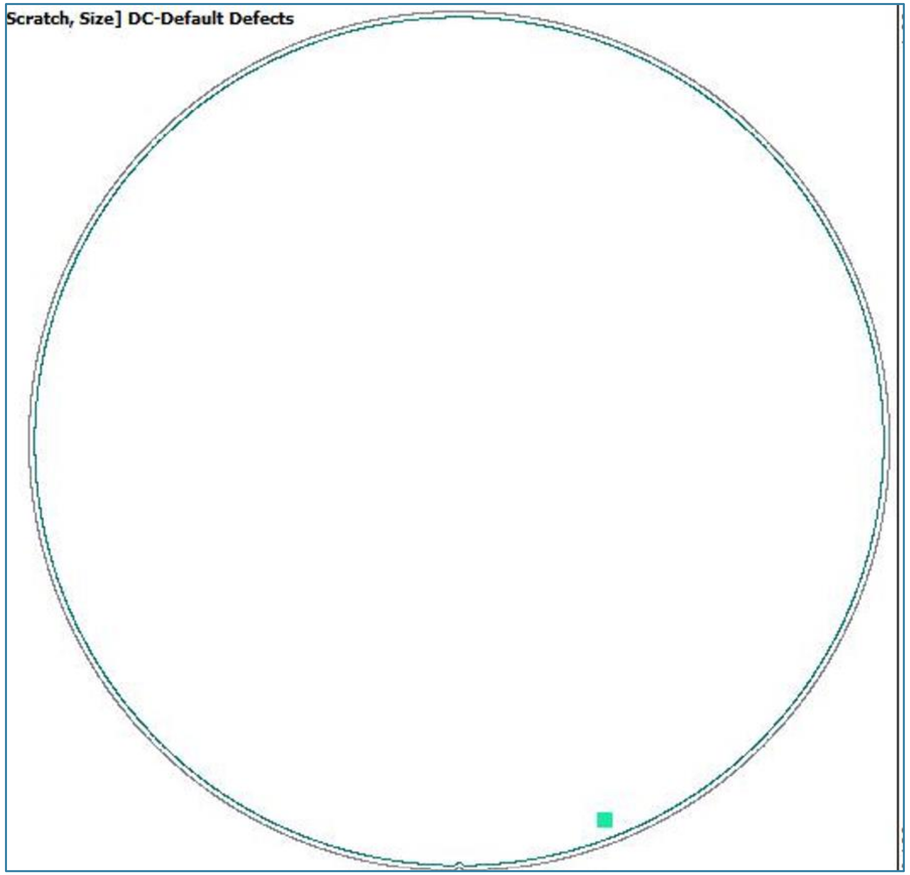
Key Takeaways and Summary

- Modern semiconductor manufacturing requires high productivity and stringent limits on defects (metals, particles) generated by all processing equipment, including ion implanters
- Increased productivity and reduced defects drives advanced ion source design and chemistry
  - Fast recipe transitions
  - Increased beam current
  - High ion source lifetime
  - High ion species purity
  - Low glitches, smooth ion source operation



DC-Default Defects Added LPD Size				
3	0.0190	-	0.0260	0
4	0.0260	-	0.0350	0
5	0.0350	-	0.0450	0
6	0.0450	-	0.0600	0
7	0.0600	-	0.0750	0
8	0.0750	-	0.0900	1
9	0.0900	-	0.1200	0
10	0.1200	-	0.2091	0
Total				1

19 nm defect free post defect map Adder: 1

Defect free can be achieved by carefully partitioning of each component and assembly with good housekeeping practice!

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