# **ECFA DRD7 Expression of Interest**

# **Common interface ASIC for detector readout, timing, and control**

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## Introduction

We propose the specification, design, and (at a later stage) fabrication of a common interface ASIC for particle detectors. This device would couple a range of specialised front-end ASICs to a common industry-standard off-detector interface. The functionality would include:

* Presentation of an industry-standard interface and protocol (IP on 10 / 25 / 100 GB/s Ethernet) for detector readout, control, and synchronisation systems
* Presentation of standardised short-haul asymmetric control / data links to front-end ASICs
* Aggregation and deep buffering of data allowing a range of efficient readout schemes and transfer protocols
* A scalable, flexible, software-programmable processing fabric allowing a range of data processing, reduction and compression algorithms to be carried out on-detector
* An SEU-tolerant watchdog subsystem ensuring autonomous recovery of higher-level functions without the necessity of hardening of all logic.

This development combines and builds on previous general and experiment-specific projects targeting standardised approaches to control, readout, and timing (e.g. GBT, White Rabbit, IPbus, FELIX, DUNE Ethernet readout, and various ‘glue logic’ ASICs), while also providing a flexible common platform for testing of advanced on-detector data reduction algorithms. The proposed ASIC (or more likely a family of ASICs sharing a common architecture but varying in processing and buffering capacity) must be flexible enough to enable a wide range of future detector applications and have sufficient low cost and power requirements.

## Motivation

This development addresses the following issues:

* The large number of similar but incompatible ASIC control and readout interfaces used in current experiments and detector R&D efforts
* Parallel developments of relatively complex control and readout logic for several applications, which has proven to be difficult to adequately test before production
* The need for higher-performance short-haul data links
* The need for intelligence and high-performance data processing on detector, without the unacceptable risk of hardwiring complex algorithm logic
* Exploitation of new capabilities offered by the deep buffers available in next-generation technology nodes
* The ability to employ a variety of readout strategies for a detector subsystem (e.g. triggered vs non-triggered) depending on experimental conditions or physics goals
* The adoption of industry-standard interfaces for off-detector electronics, and the resulting simplification of control and readout software.

In addition to these technical objectives, the development of a scalable all-digital SoC ASIC in an advanced technology node (i.e. 28nm) will provide an appropriately exemplar project for the community, complementing work already being done to characterise analogue and mixed-signal blocks in new processes. A flexible SoC architecture allowing incorporation of several types of processing elements – ranging from general purpose CPU cores based on commercial IP, through SIMD cores, to custom fixed- or programmable-function data manipulation engines – will provide a test case for new approaches to sharing of IP and common design, simulation, and optimisation tools.

## Architecture

A simplified outline architecture is shown in the figure below. Appropriate design approaches should allow a similar architecture to be used for a range of possible devices with parameters as follows:

* Number and bandwidth of data links and Ethernet interfaces
* RAM buffer and bus fabric capacity and bandwidth
* Number and type of processing cores



The main architectural features are:

* **RAM buffer**, used to hold event data and intermediate data products while waiting for readout requests. In reality, it is likely that the buffer would be segmented into a low-performance / high-capacity buffer versus high-performance / low-capacity scratchpad, and that additional local / cache RAM will be needed to sustain adequate performance.
* **Processor array**, comprising a mixture of general- and special-purpose cores and / or programmable logic arrays. The performance of individual cores will necessarily be low compared to current-generation commercial CPUs but should be comparable with medium-performance embedded CPUs. Customisation of CPUs and / or extension with specialised logic or additional instructions will increase performance for this specific ‘stream processing’ application.
* **DMA engines**, to allow efficient and semi-autonomous data movement to and from the buffer.
* **Datalink interfaces**, receiving raw or packetized data from front-end ASICs via a standardised high-bandwidth uplink, and providing control and timing information on a low-bandwidth downlink.
* **Watchdog / configuration subsystem**, providing monitoring, isolation, and recovery of other elements if affected by SEU. This subsystem will be fully SEU-hardened, and operate from ROM.
* **Clock recovery block**, using a White-Rabbit-like combination of synchronous Ethernet frequency reference along with a higher-level protocol for timestamping and delay calibration. Dedicated timing calibration interfaces may also be needed where highly precise phase alignment is required.
* **Bus fabric**, interlinking memory and processing elements.

It is likely that advanced emulation and hardware / software co-simulation tools will be required to properly estimate the performance of different architectural choices, and this can directly build upon the growing experience in the user community in use of advanced processing platforms (e.g. GPU, FPGA, SIMD, ‘AI cores’) in offline computing.

## Example applications

### Calorimeter readout for e+e- detectors

The calorimeter subdetectors of the future e+e- experiments will have varying requirements for readout architecture and on-detector data processing, depending on:

· Running mode (e.g. H factory vs Z pole running)

· Detector occupancy as a function of polar angle

· Detector granularity and readout volume as a function of position

· The requirement for precision timing information, e.g. depending on the content of corresponding tracking system data

This requirement could be accommodated with a single readout ASIC / interface ASIC combination, by tailoring *a priori* the data density per interface ASIC, but altering *in situ* the readout strategies and / or data processing algorithms by reprogramming the processing fabric.

### Distributed photon readout for neutrino / DM detectors

Future neutrino / DM detectors are likely to incorporate very large arrays of single-photon-sensitive detectors operating under cryogenic conditions. Cost-effective implementation of this approach requires (a) minimal logic and power dissipation in the cold volume, (b) an efficient approach to local and regional data reduction, (c) a highly multiplexed readout architecture to take advantage of the low occupancy. Progress in this area for distributed charge readout has already been made, e.g. by the LArPix collaboration. This can be further enabled by combining specialised cryogenic front-end ASICs hybridised with SiPM arrays, with the common interface ASIC in the warm for data reduction, buffering, and triggering. In this application, an on-detector Ethernet network would allow extreme levels of data multiplexing and even event-building functionality without the need for substantial traditional computing capacity in a hostile environment.

### Standardised test-beam readout

The idea of a single uniform software suite to provide readout for a variety of detectors has been the goal of several R&D projects in the past but falls apart when confronted with the large variety of complex control / readout / timing interfaces integrated into modern sensors and ASICs. The factorisation of this functionality into a common and custom part will greatly simplify several layers of the necessary software stack, also allowing scalability from small prototypes to full detector subsystems. The use of Ethernet as the readout link standard will also allow debugging using commodity computing equipment (laptops…) in the lab. For this application, cost-optimisation of the ASIC will be important.

## Project approach

**Stage 1:** Architectural definition and estimation of required / obtainable performance and ASIC parameters (gate count, cost, power requirements technology, availability and cost of IP blocks). Investigation of candidate use cases based on requirements of other DRDs. ~1 year.

**Stage 2:** Definition of link specifications and protocols, implementation of test algorithms in FPGA-based test platform. Development of emulation tools. Trial implementation and simulation of key ASIC blocks using selected toolset. Detailed specification of interfaces allowing design into prototypes. ~2 years.

**Stage 3:** Previous stages bring us to the end of a 3 year period of work establishing specifications and developing the circuit blocks and software for Stage 3, to design and implement a minimally-configured ASIC (including programmable data sources representing front-end ASICs) and test as part of R&D programme. ~2 years

Work Package Breakdown

WP 1: Definition of requirements

A study of candidate use cases based on requirements from other DRDs in order to establish goals and steer architecture development.

WP 2: Emulation and architectural studies

This work package will build on the groundwork carried out by the CERN team within the EP R&D activity (WP5: IC Technologies), investigating Rad-hard processor IP, SoC architecture and Application Specific Instruction set Processor design. The CERN team’s work will guide the approaches employed here and will link directly with their proposal to continue their developments under DRD 7.2.

WP 3: Datalinks & Ethernet

Link IP will be developed in collaboration with others in DRD 7.5.

WP 4: Clock recovery and timing distribution

This work package will work closely with activities under both DRD 7.3. to establish an agreed approach to system timing distribution.

WP 5: Processor cores and Memory

This work package will build on the groundwork carried out by the CERN team within the EP R&D activity (WP5: IC Technologies), investigating Rad-hard processor IP and ASIP design and will link to their developments under DRD 7.2.

WP 6: ASIC Assembly and Configurability

This will cover the top-level ASIC digital-on-top flow for assembling the full ASIC and enabling future configurability for a possible chipset that can be tuned to experiment requirements.

WP 7: Software tool chain for cores

This task will include a survey of available tool chains to explore the likely split between vendor-specific and open standards.

WP 8: Back-end software libraries and test software

This work package will survey existing use cases to establish the needed general functional blocks to facilitate both low level testing, with detector-specific processing, as well as integrating with larger scale systems. The work should include an assessment of commodity/open source software currently available with focus on suitability and longevity

WP 9: ASIC SoC Verification

A Universal Verification Methodology (UVM) wrapper will be developed in collaboration with WP 1, to ensure that the ASIC performance against expectations is verifiable at every stage of development.

WP10: Hardware Testing

Both IP developed in the project and the final prototype ASIC will require the development of test platforms.

Estimated effort

Based on previous developments of this type we are looking at between 50-75 staff-years or between 10 and 15 people active on the project over five years.

The most likely scenario is a ramp up of effort through the initial phase, with some variability over the course of the project.

Flexibility will be needed to accommodate for project dependency on contributions from external groups.

R&D framework and funding

Within the UK this activity is expected to be funded as part of a UK Strategic Detector R&D Programme. International collaborators will be required to seek funding from their national funding agency.

Dependencies

* Effort and timescales for the ASIC implementation will depend on the availability of IP blocks and the availability of effort from participating international partners.
* Any IP licensing Ts & Cs and cost.

Deliverables

* **Stage 1** (*End of year 1*)
	+ Specification of architecture and performance requirements
	+ Survey of IP block availability
	+ Definition of IP blocks for development
* **Stage 2** (*End of year 3*)
	+ IP blocks – Links, SoC components, etc.
	+ Emulation of chosen system architecture (Software & Hardware)
* **Stage 3** (*End of year 5*)
	+ A minimally configured prototype ASIC manufactured on a TSMC 28nm.
	+ Software tool chain for cores
	+ Back-end software libraries

Contributors

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| **Institute** | **Name** | **Competency** |
| STFC - RAL | Dr William Buttinger | Research Physicist -- Experienced in test and control software as well as statistical analysis techniques for HEP. |
| Mark Prydderch | ASIC Design Group Leader – Experienced in the development of Front-end microelectronics for detector systems. |
| Dr Alessandro Thea | Senior Scientist -- DAQ and tracking expertise. Technical Lead of the Data Acquisition and Slow Control consortium of the DUNE experiment. |
| Dr Thomas Williams | Research Scientist -- Experienced in control and monitoring software, firmware and system testing. Phase-2 upgrade integration coordinator for the CMS level-1 trigger. |
| Royal Holloway, Uni. Of London | Dr William Panduro Vazquez | Senior Research Officer - experience with the development of commodity readout in ATLAS, previously leader of the FELIX project, now leads the ATLAS TDAQ Upgrade for HL-LHC. |
| Uni. Of Manchester | Dr Conor Fitzpatrick | Physicist – Former LHCb HLT Project Leader, current LHCb Upgrade 2 Real-Time-Analysis R&D coordinator. |
| Uni. Of Warwick | Dr Karolos Potamianos | Physicist (Assistant Prof) – Experience with the characterization, commissioning, and operation of silicon detectors. DAQ and tracking expertise. |
| Uni. Of Birmingham | Dr Karol Krizka | Assistant Prof. Particle Physics Instrumentation -- Experienced in digital logic design, ASIC bench-top testing (including radiation hardness) and development of test systems (software & electronics). |
| Uni. Of Bristol | Dr Jim Brooke | Senior Lecturer – Experience with firmware and software processing, control software, simulation and commissioning in context of back-end systems, in particular CMS L1 Trigger and DUNE DAQ. Co-lead for DAQ within DUNE UK. |
| Dr David Cussans | Research Fellow – Experience in custom electronics design for detector readout and DAQ. Experience of commissioning detectors in wide range of experimental contexts. Current lead for DUNE Timing System. |
| Dr Sudarshan Paramesvaran | Senior Lecturer – Experience in backend systems - DAQ and L1 Trigger design, implementation, installation, and commissioning. Experience in designing and running integration programmes for back-end systems. Former CMS Run coordinator & L1 Trigger Upgrade technical coordinator. |

Contributions to DRD7 Proto-projects

WG 7.2 – Intelligence on the detector

* Interested in contributing to proto-projects (a), (c) and (d). Specifically, evaluation of reduction techniques and system-level architecture modelling.
* Software, DAQ and ASIC expertise.
* Estimated effort: 3 FTE
* Funding to be requested this year for a minimum of 5 years.

WG 7.3 – 4D and 5D techniques

* Interest in contributing to proto-project (c). Specifically, IP for timing distribution of Common Interface ASIC.
* ASIC and DAQ expertise.
* Estimated effort: 4 FTE
* Funding to be requested this year for a minimum of 5 years.

WG 7.5 – Backend Systems and COTS

* Interest in contributing to proto-project (c). Specifically, the development of Ethernet, Clock recovery and Versatile Short-haul links.
* Software, DAQ and ASIC expertise.
* Estimated effort: 6 FTE
* Funding to be requested this year for a minimum of 5 years.

**NOTE:** The effort estimated here is likely to be a mix of full-time staff, academic staff and PhDs, the make-up of which is yet to be determined.